Intel Developer Forum Spring 2002

Breaking Barriers to Moore's Law

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Intel Labs

http://intel.com/labs

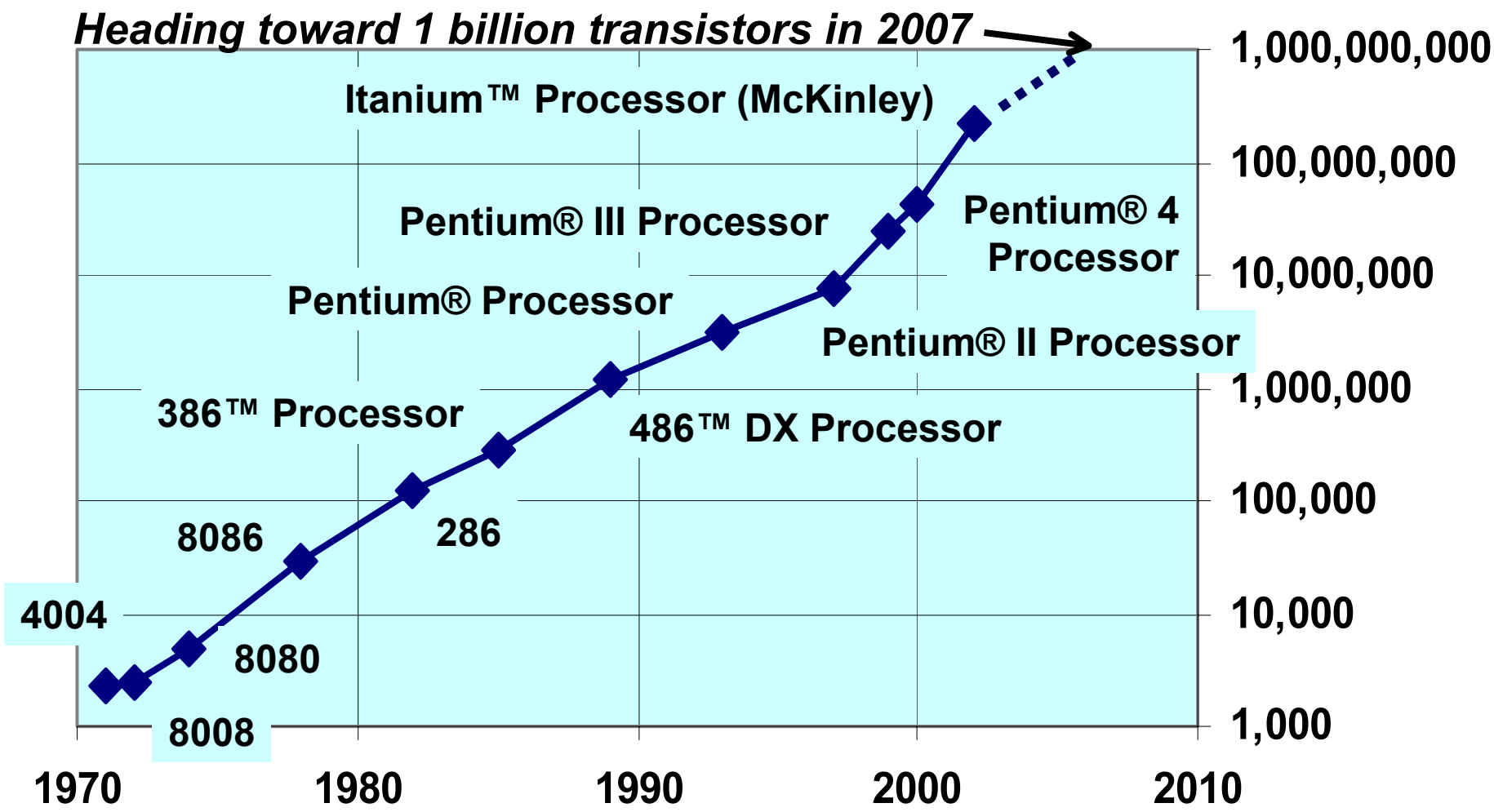
Outline

- Introduction
- Manufacturing
- Lithography
- Transistors
- Packaging

Our environment

- Increasing chip manufacturing complexity
- Increasing global development and manufacturing
- Continuing cost control efforts
- Increasing environmental regulations
- Growing concern about power consumption

Moore's Law



How does Intel operate in this environment?

- De-Centralized Research Groups
- Centralized Silicon Wafer Development
  - Logic: Hillsboro, Oregon
  - Memory: Santa Clara, California
- Copy Exactly! from development into manufacturing
  - Multiple factories, multiple countries

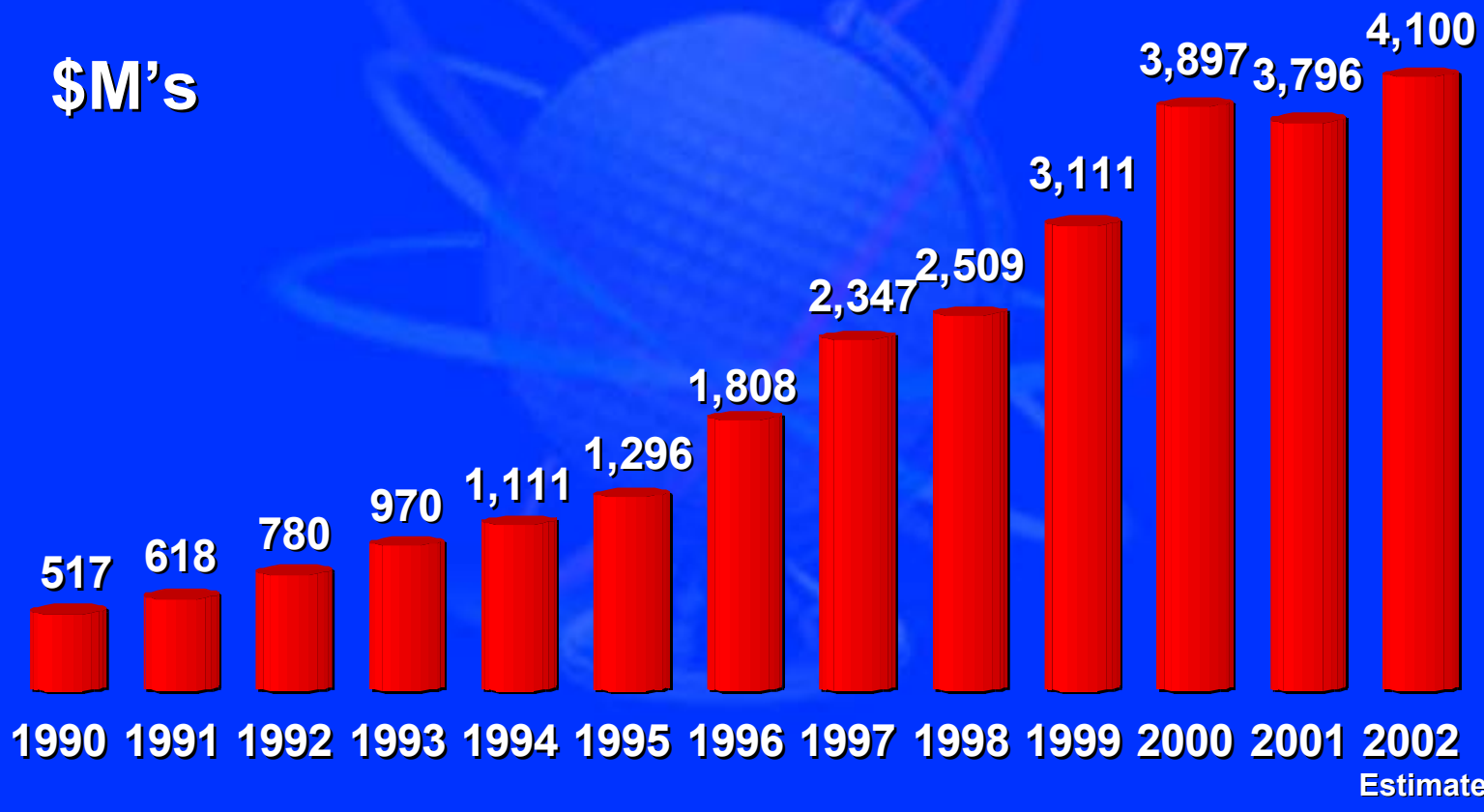
Moore's Law Drives Research, Development & Manufacturing

- New technology generation every 2 years
  - 2x die per wafer with ½ transistor cost
  - 2x microprocessor speed
- Flawless ramp of new technologies into high volume manufacturing (HVM)
  - High yields, cost-effective manufacturing
- Introduce new products during HVM ramp
  - Deliver best products on the best technology

Process Evolution

	Actual				Forecast		
Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268
1st Production	1997	1999	2001	2003	2005	2007	2009
Lithography	0.25	0.18 µm	130 nm	90	65	45	32 nm
Gate Length	0.20	0.13 µm	65 nm	45	32	22	16 nm

Huge R&D Investment



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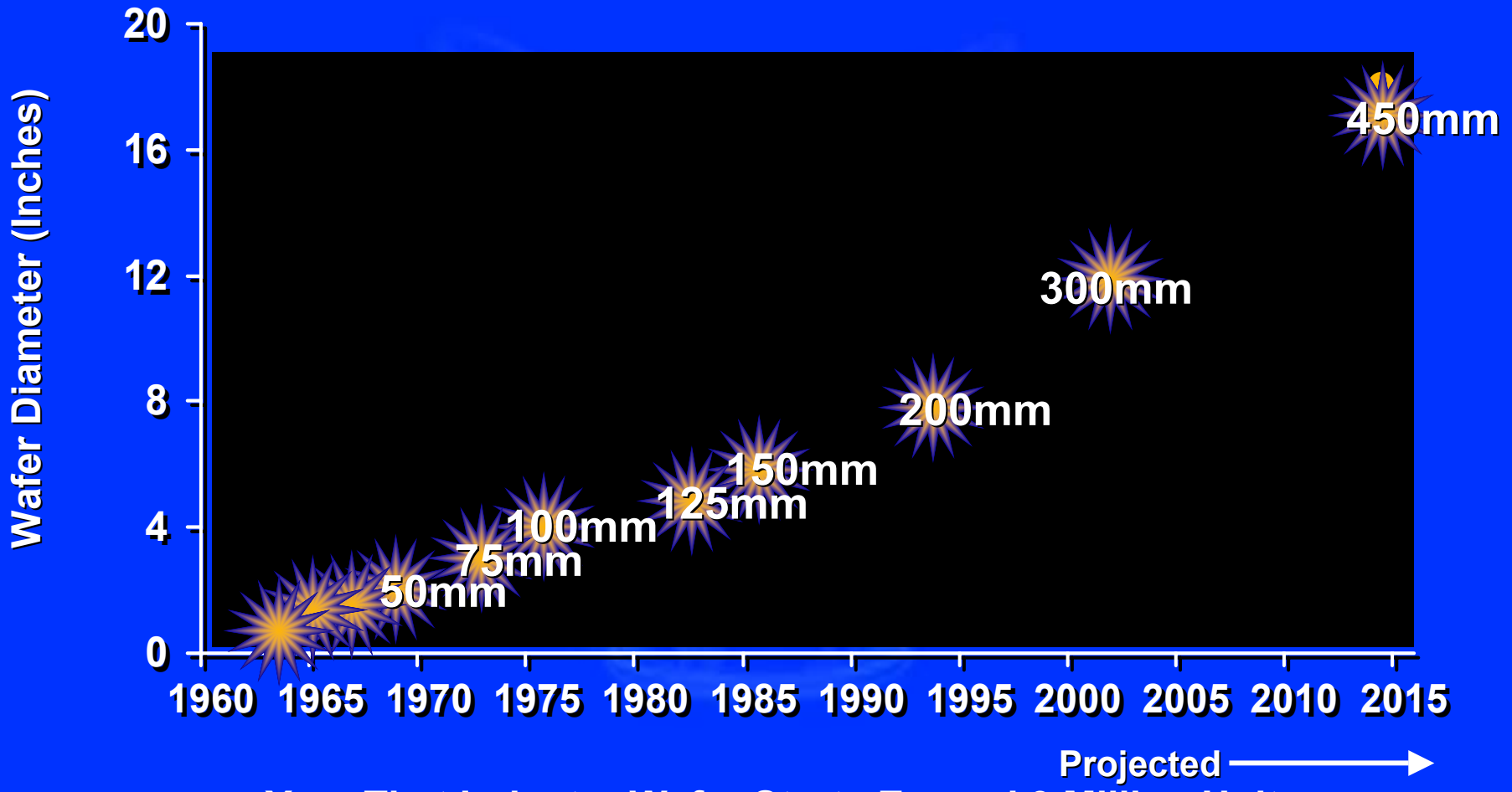
Source: Intel 2001 Annual Report

Wafer Size Transitions



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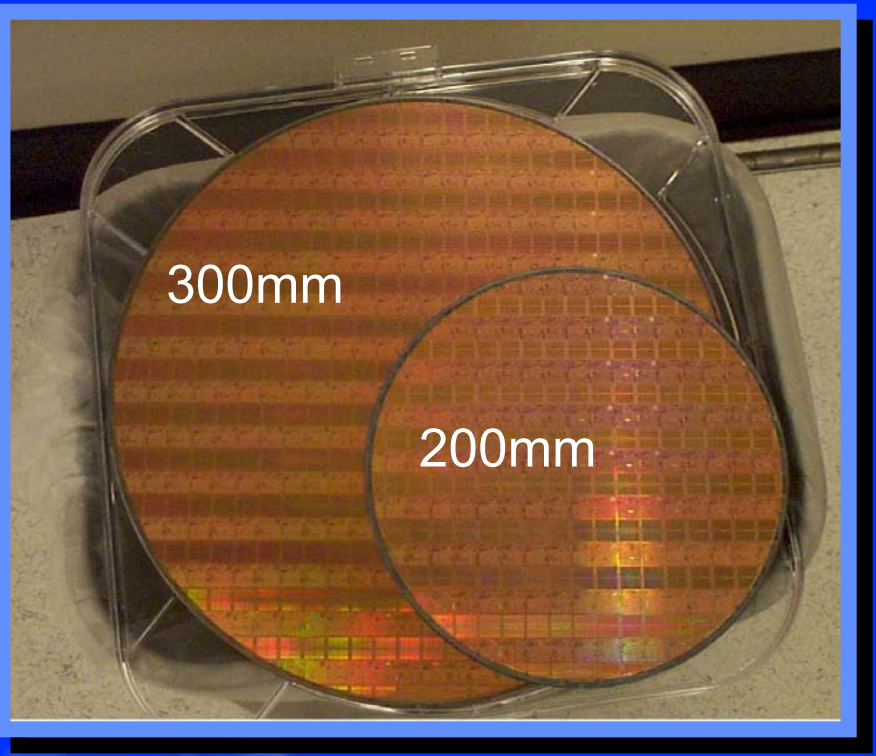
Source: VLSIR

300mm Wafer Transition

March 2001:
First fully functional 300mm wafer on 0.13µm technology



Capacity and Cost Benefits:
240% more die/wafer
30% lower cost per die
40% less energy and water per die

Moore's Law + 300mm Wafers = 4x advantage

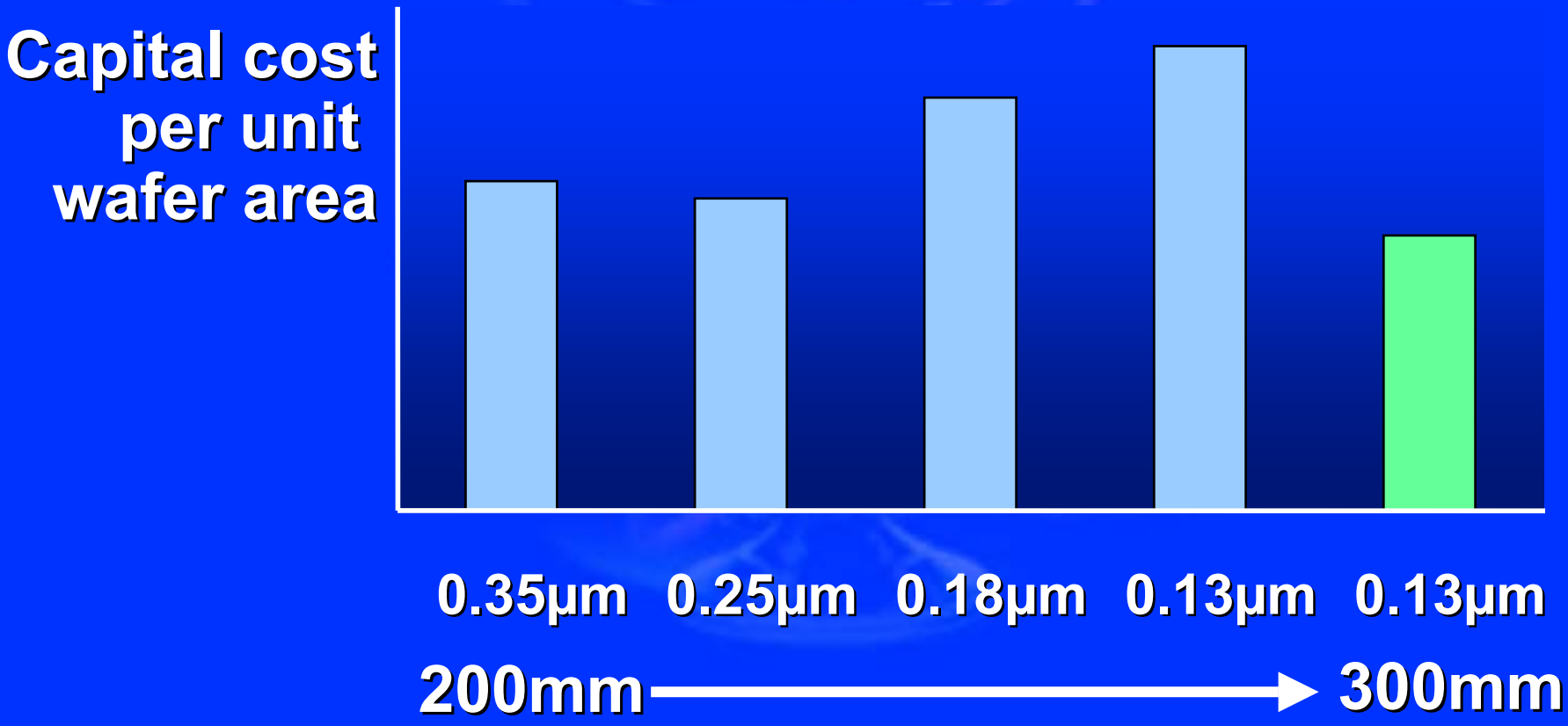
- Moore's Law:
  - From 0.18 µm to 0.13 µm = 2x transistor density
- 300mm Wafers:
  - From 200 mm to 300 mm = 2.4x silicon area
- Combined output advantage:
  - > 4x output per factory vs 0.18 µm on 200mm

300mm Automation

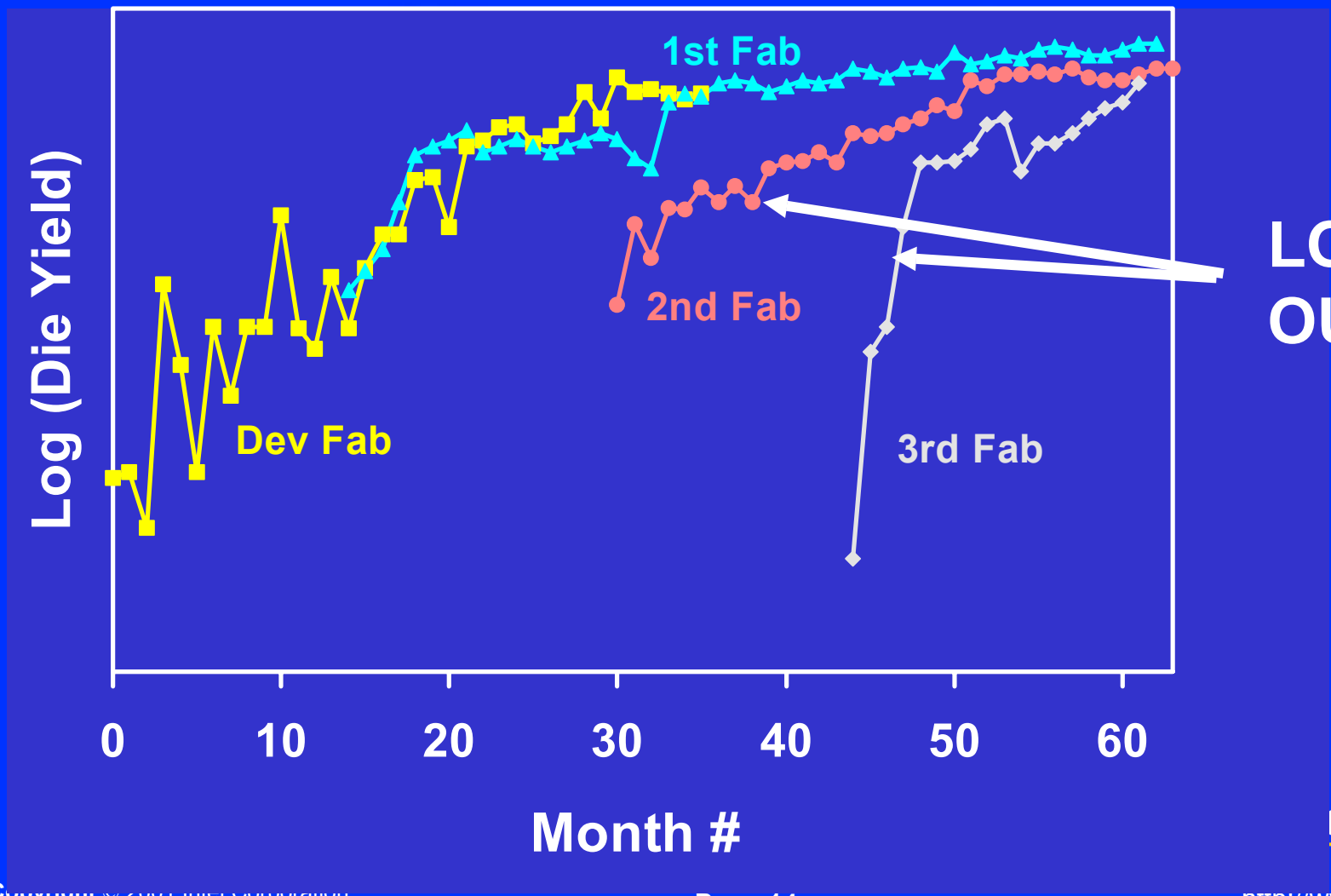
Multilevel automated material handling system

Overhead hoist vehicle (OHV) and "FOUP" (wafer box)

300mm Rolls Cost Back

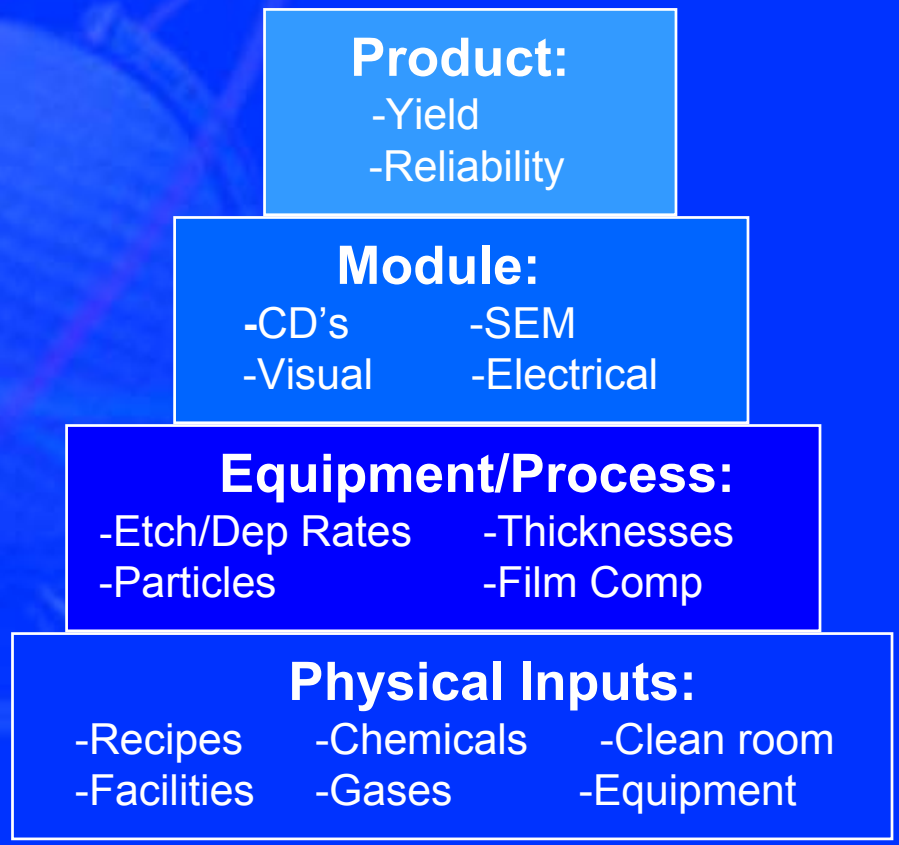


The Birth of Copy Exactly! Intel 1μm Process

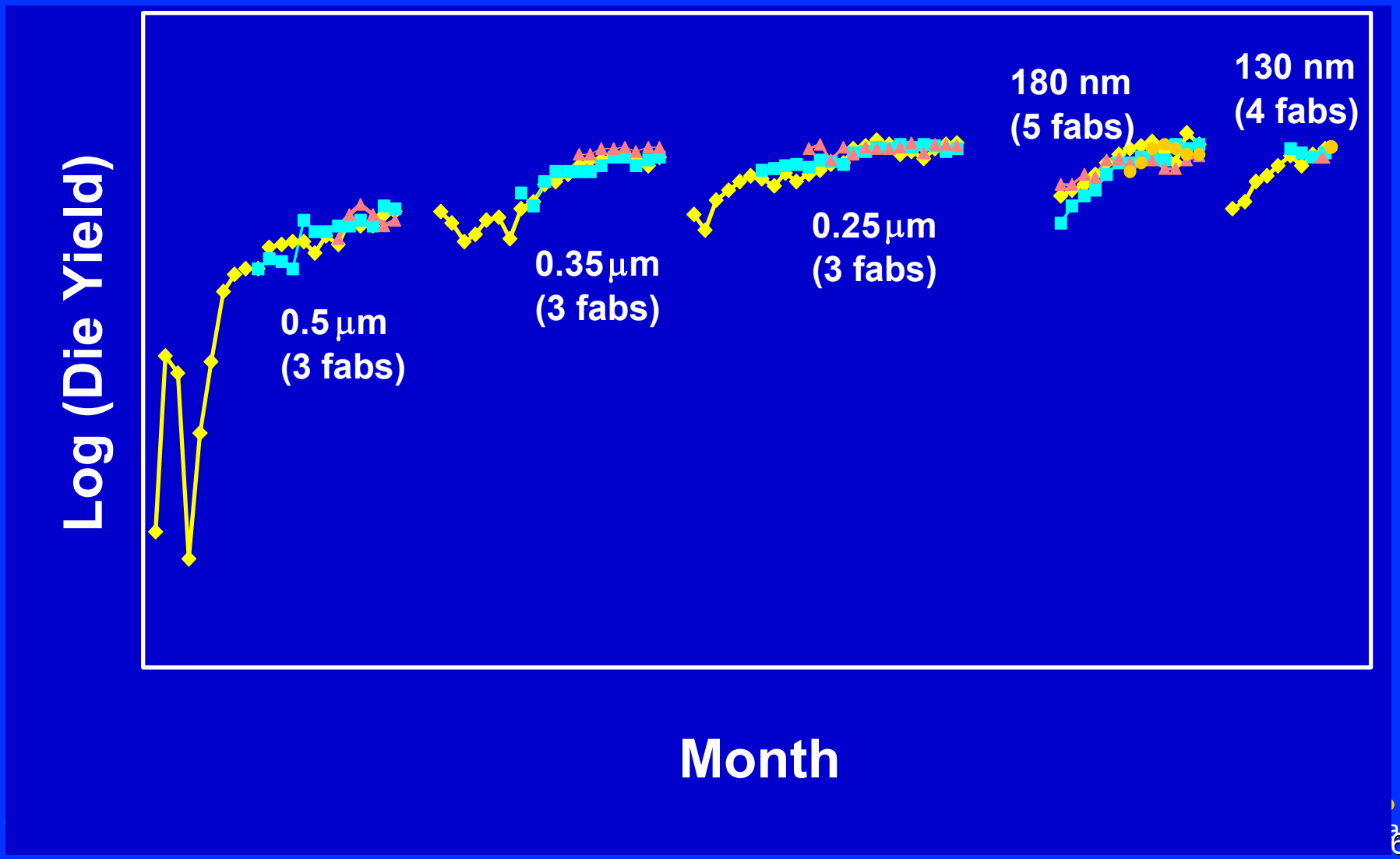


Copy Exactly! Method

- **Matching at all levels**
  - **same physical inputs**
  - **statistically matched responses (outputs)**
- **Keeping matched**
  - **coordinated changes**
  - **audits**
  - **process control system**
  - **joint fab mgmt structure**

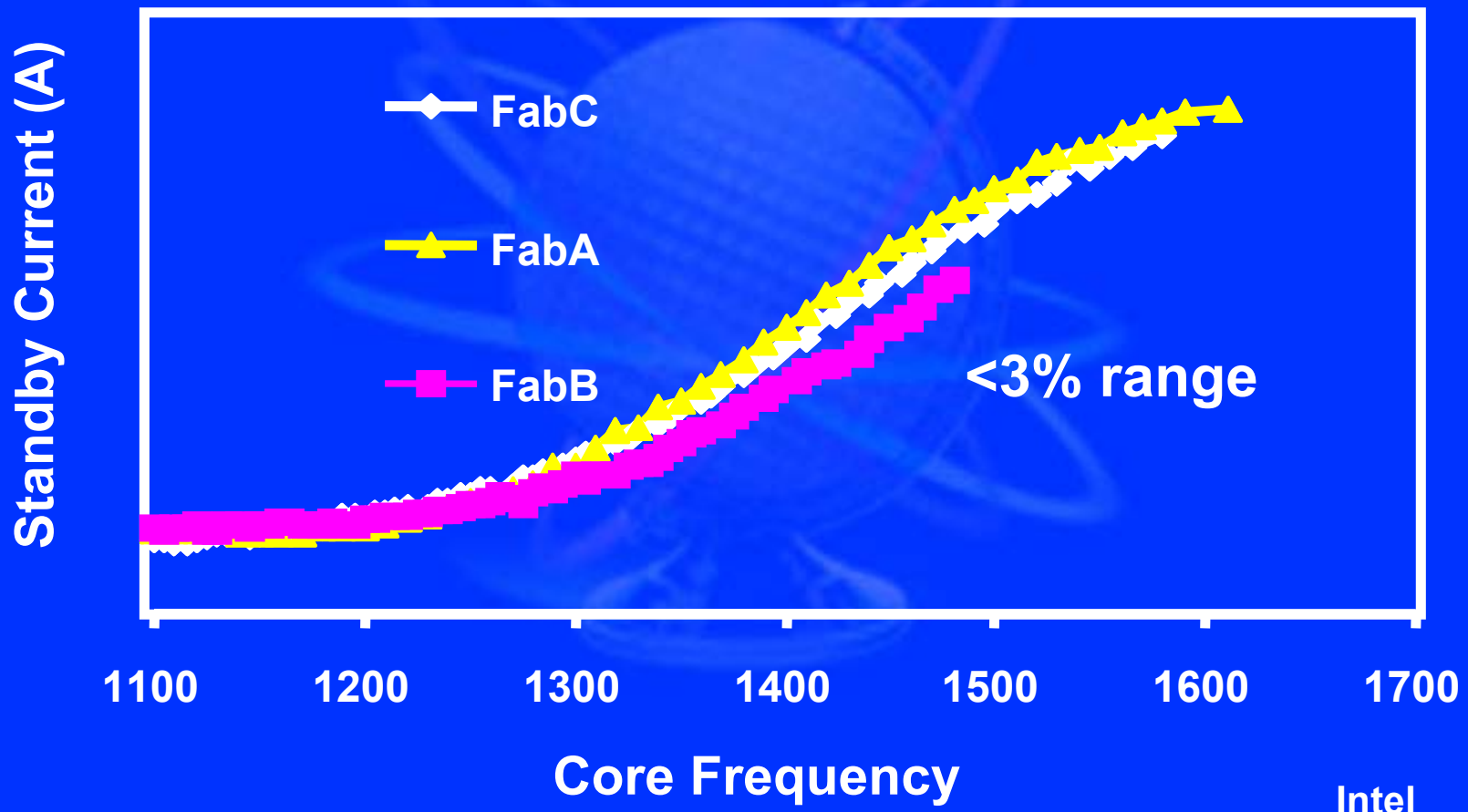


200mm Yield Matching



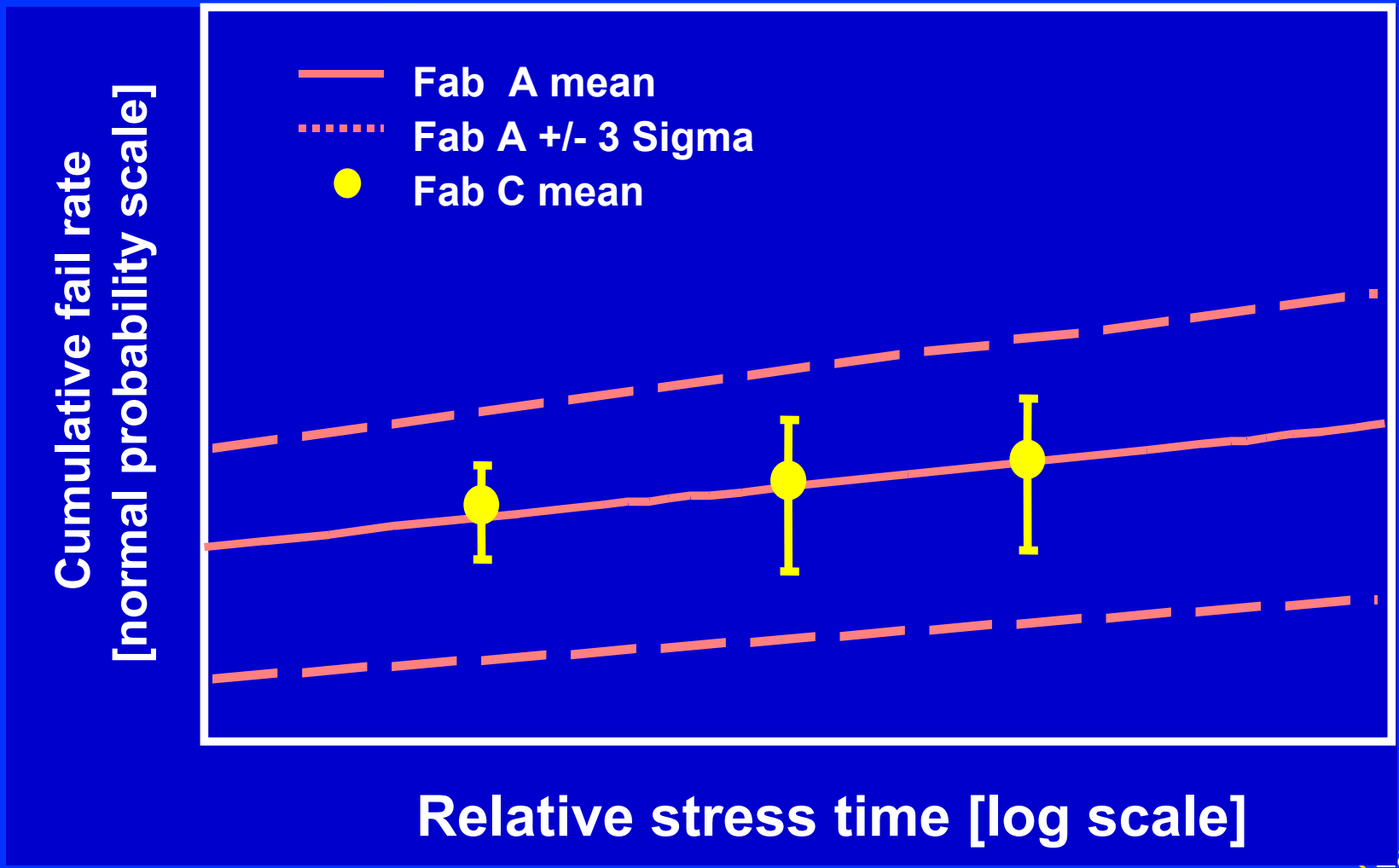
130nm Tech Performance Matching

Pentium® III processor frequency

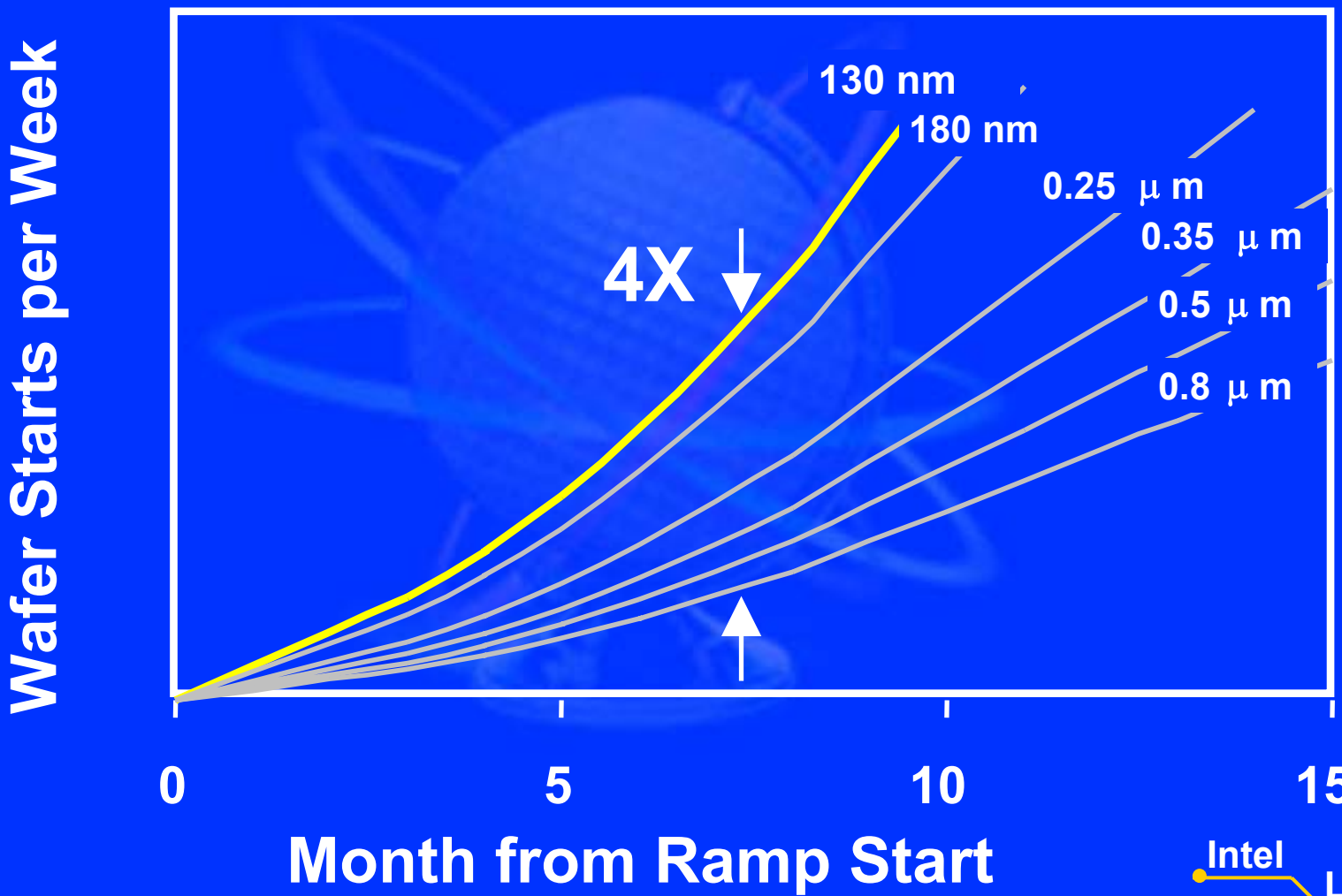


130nm Tech Reliability Matching

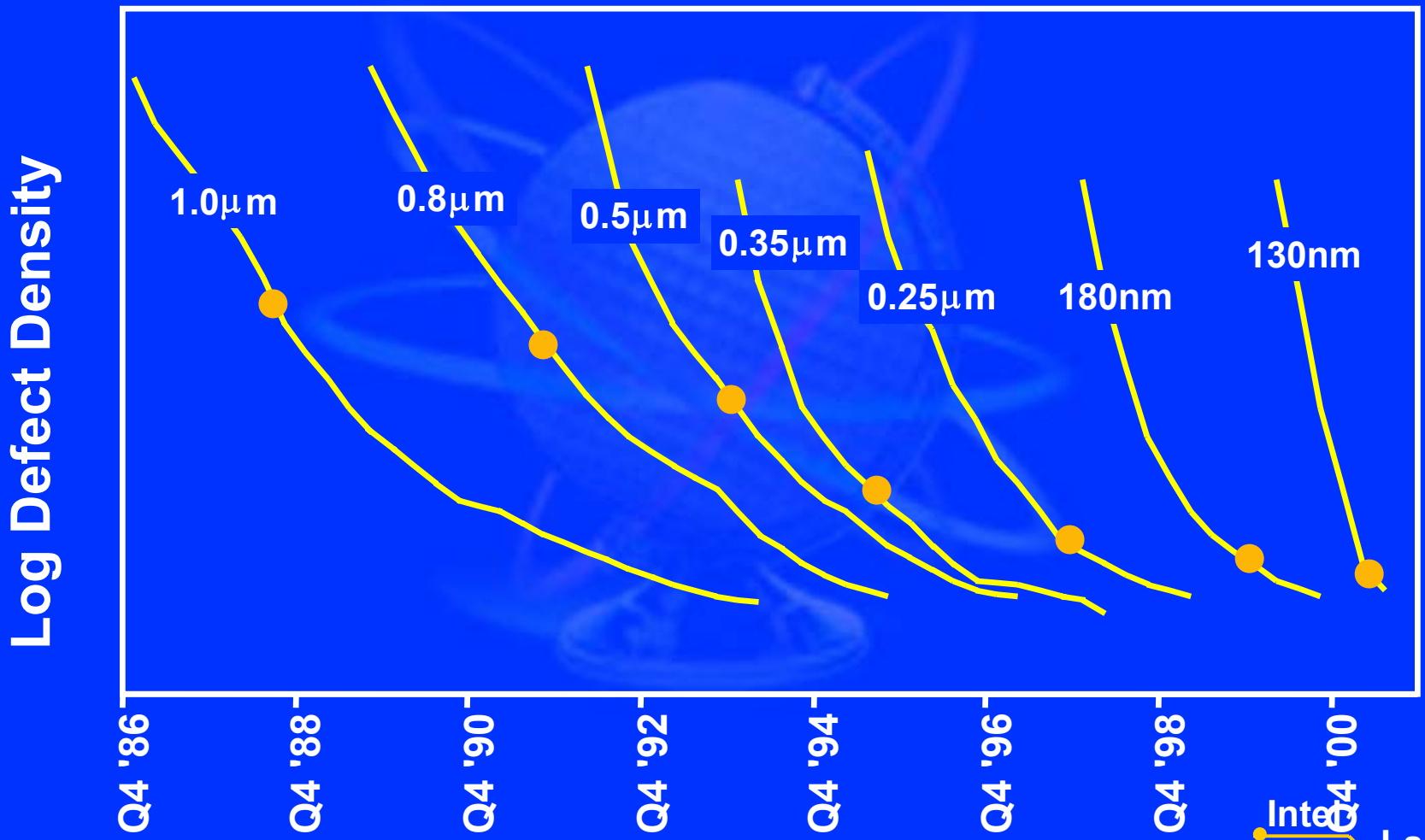
Pentium® III processor burnin



Manufacturing Ramp Rates Improving



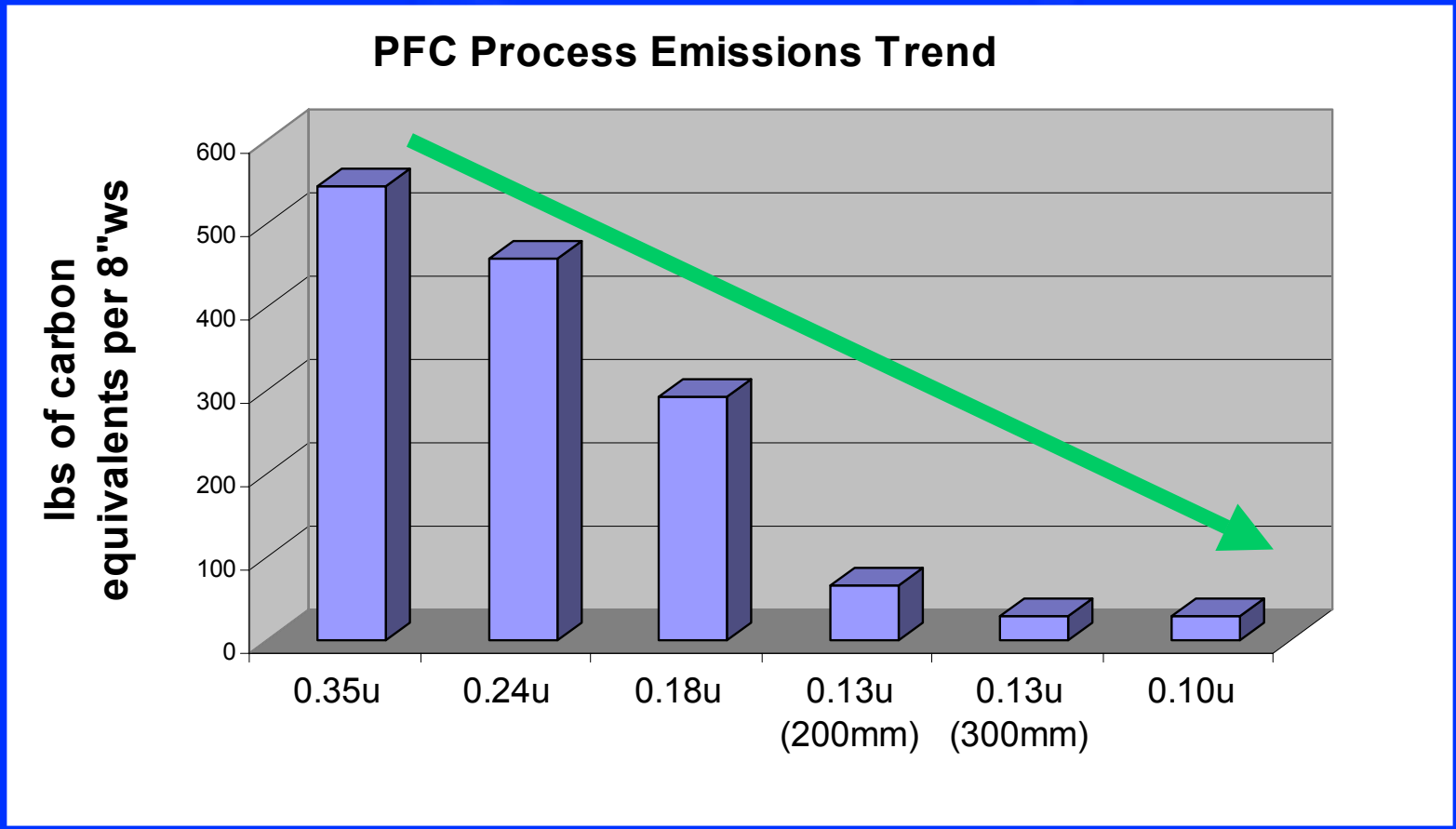
Yield Learning Rates Improving



Intel's Environmental Methodology

- Research group demonstrates feasibility of new chemicals and equipment
- Manufacturing tools, chemicals, and process recipes are finalized during development process
  - Emissions and environmental data is incorporated into the manufacturing tool selection process
- Development process is transferred using Copy Exactly! into all manufacturing sites

95% Reduction in Emissions per Silicon Area



300mm Tools are More Chemically Efficient

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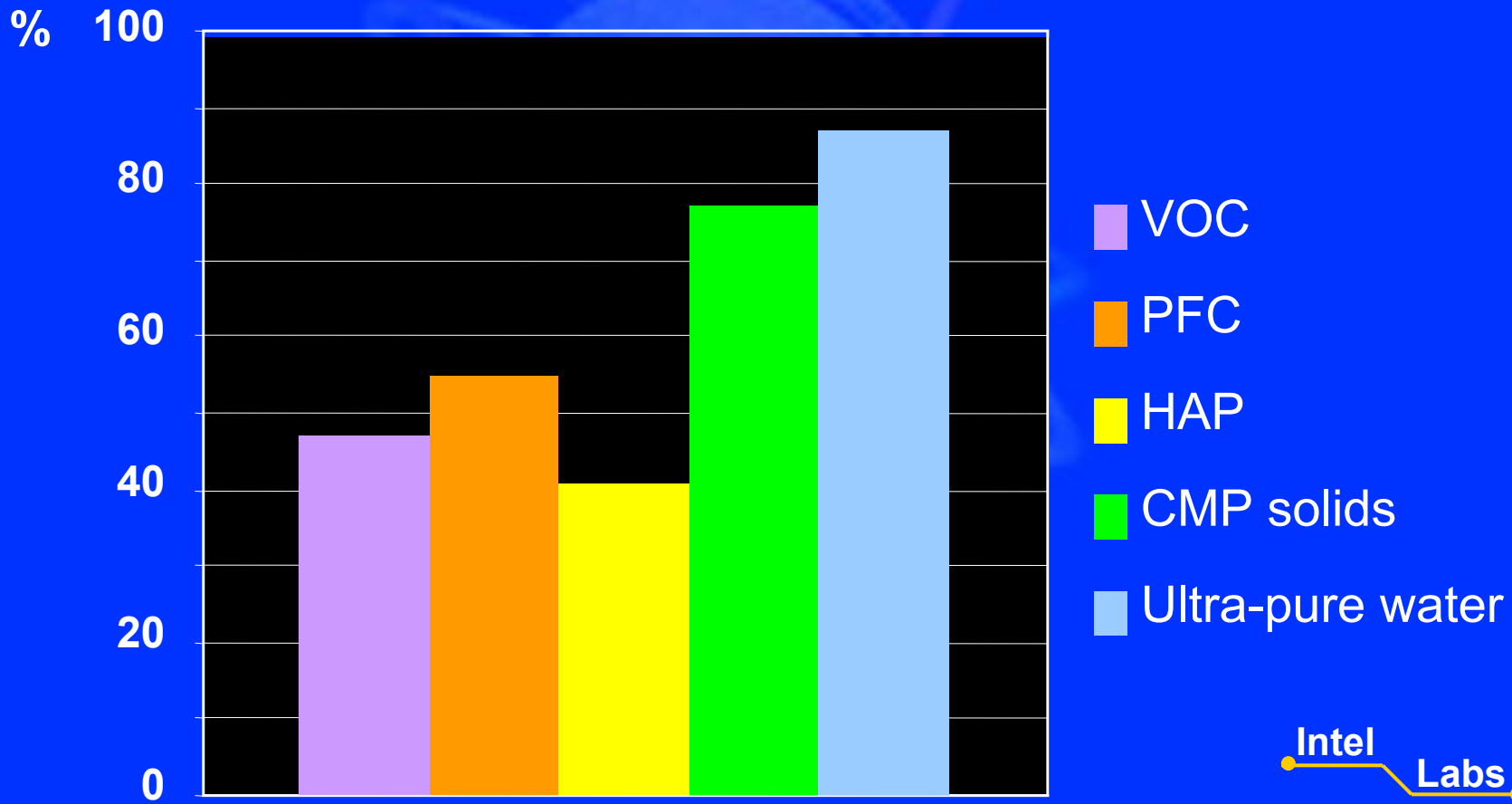
Estimated 300mm emission / consumption relative to 200mm (per unit silicon area)



Source: Vendor data

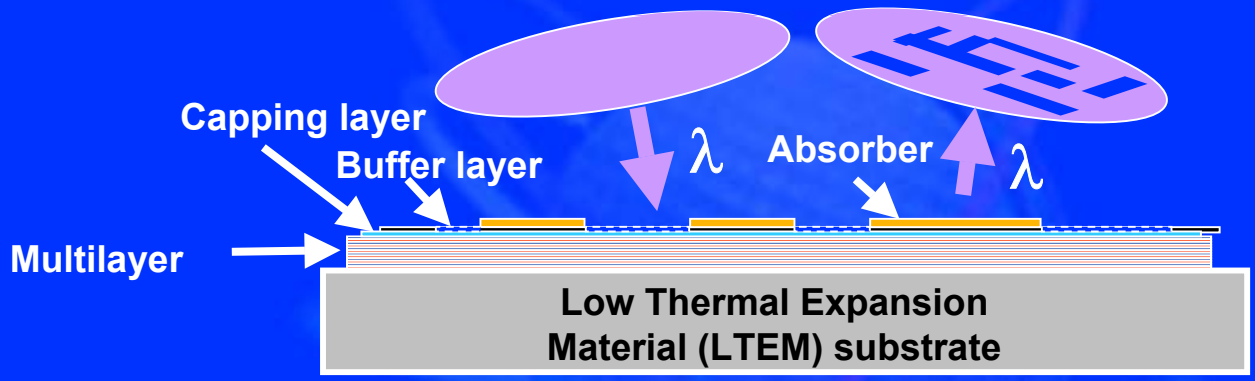
Intel Delivers

- High volume manufacturing of Intel's most advanced technologies is one of Intel's strategic advantages
- 300 mm output capacity will help distance Intel from our competitors

Lithography

- Challenge: cost effective way to print smaller dimensions
- One Research Approach:
  - Shrink wavelength of exposure light
    - 248 nm wavelength — manufacturing
    - 193 nm wavelength — development
    - 157 nm wavelength — pathfinding
    - 13 nm (EUV) wavelength — research

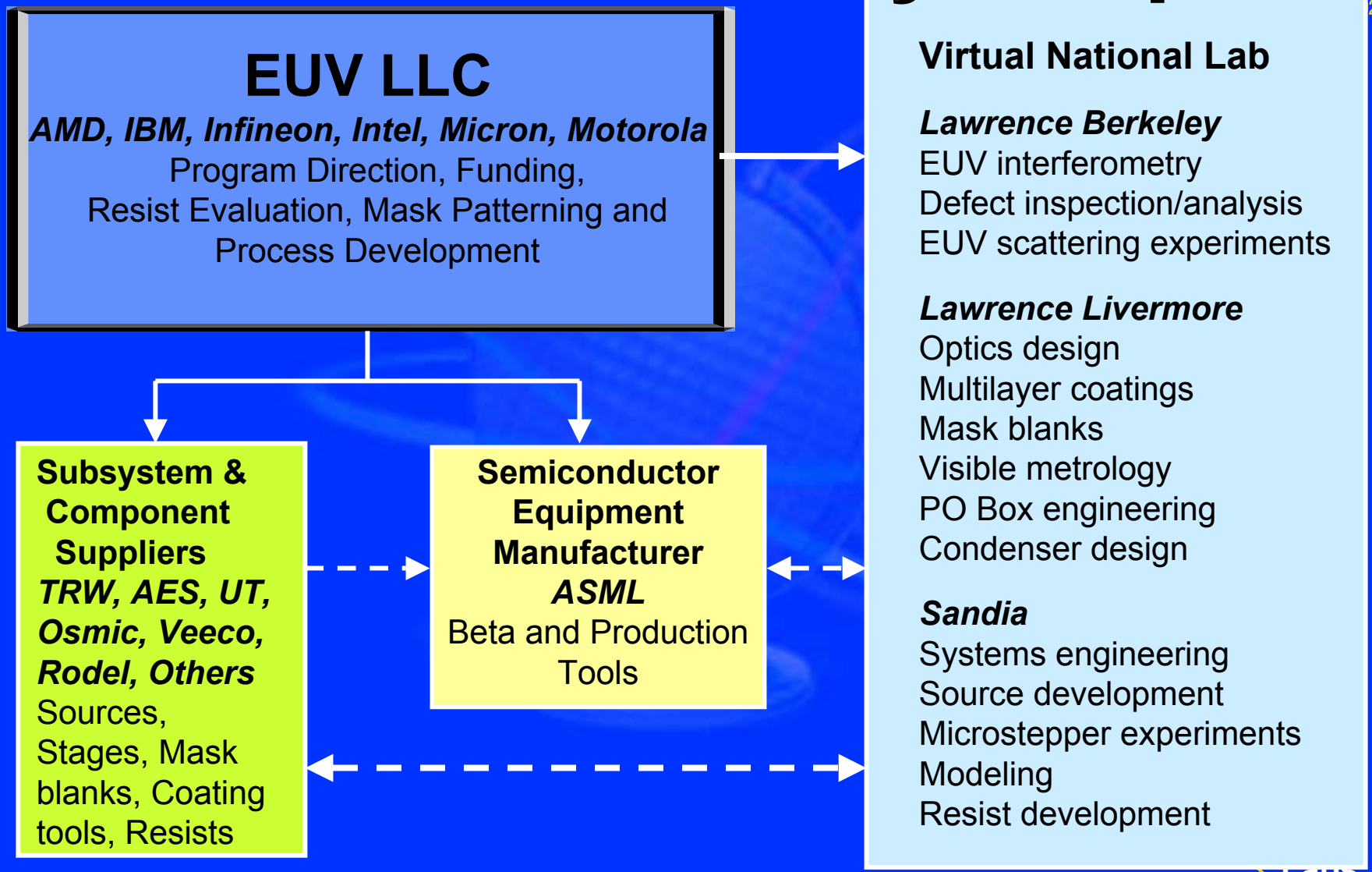
EUV is a disruptive technology



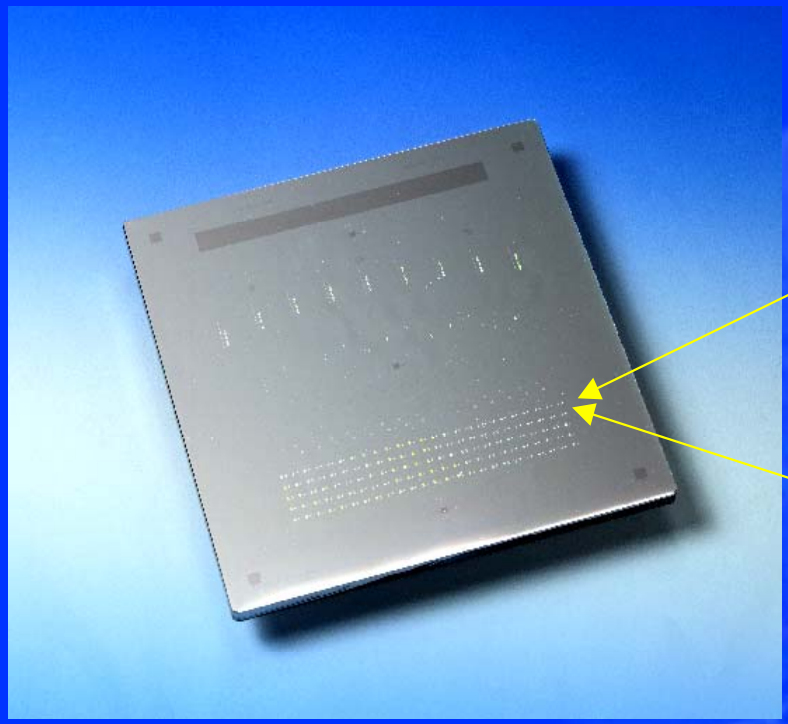
Mask Structure with incident and reflected EUV

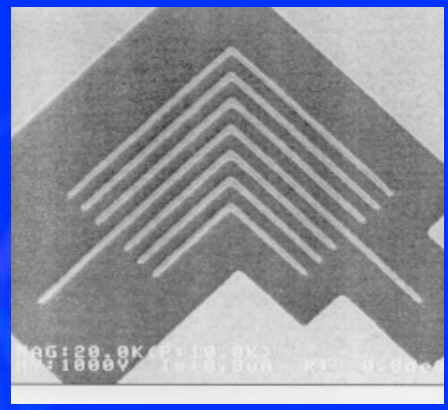
EUV light does not transmit through glass or air

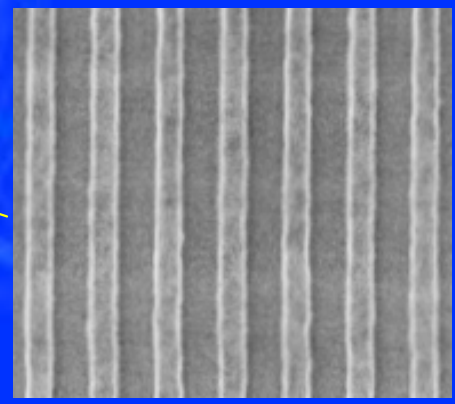
EUV Limited Liability Corp.



Intel Delivers World's First 6" EUV Mask



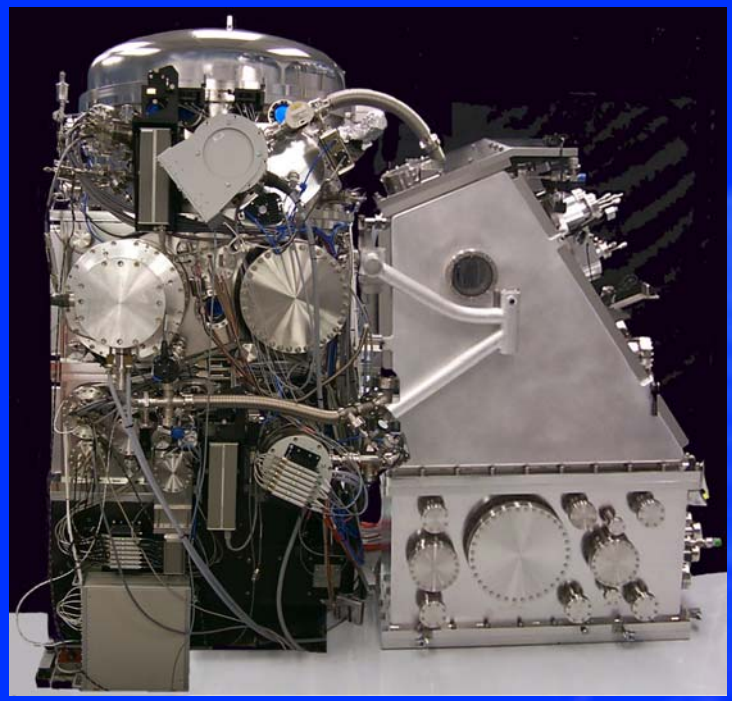




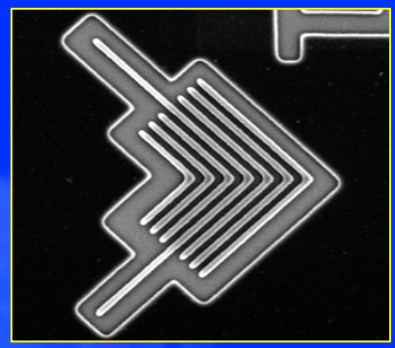
120 mm x 104 mm field size

200 nm lines/spaces for 50 nm node

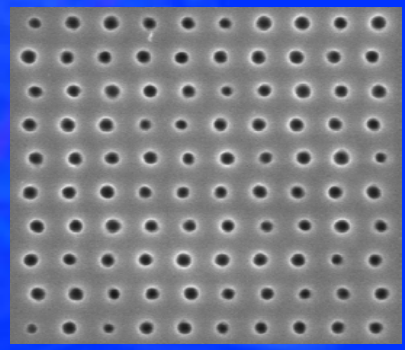
EUV Optics Upgrades



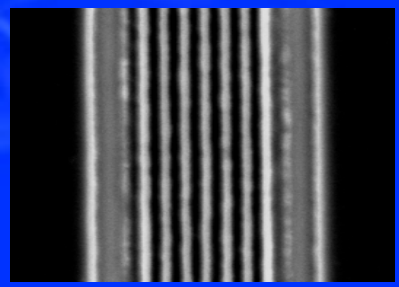
EUV Prototype in Livermore CA



100 nm
k_1 = 0.75
(σ = 0.8)

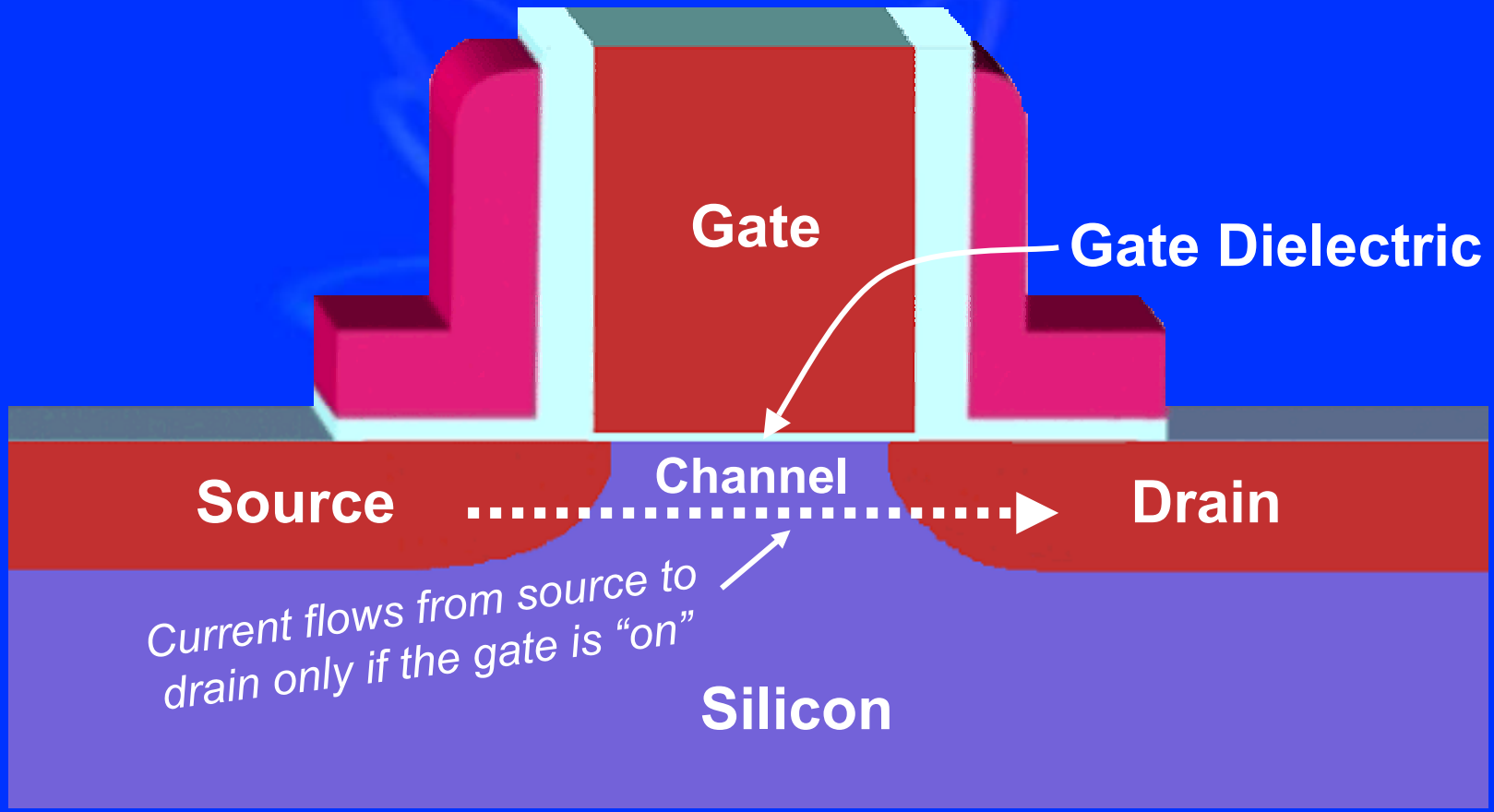


70 nm
(σ = 0.8)



50 nm dense
k_1 = 0.37,
Dipole
illumination

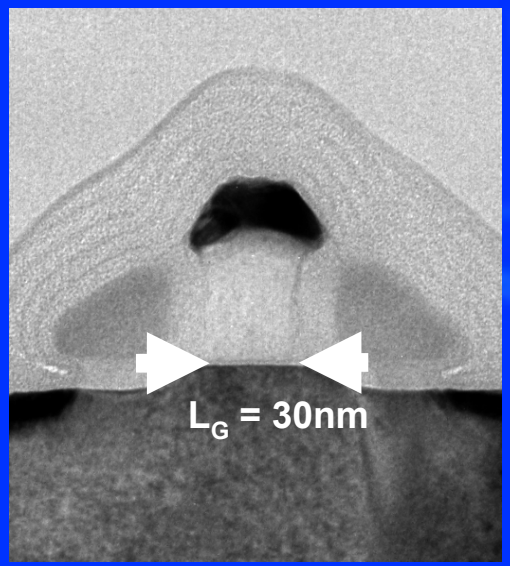
Close-up of a CMOS transistor



Transistors Keep Shrinking

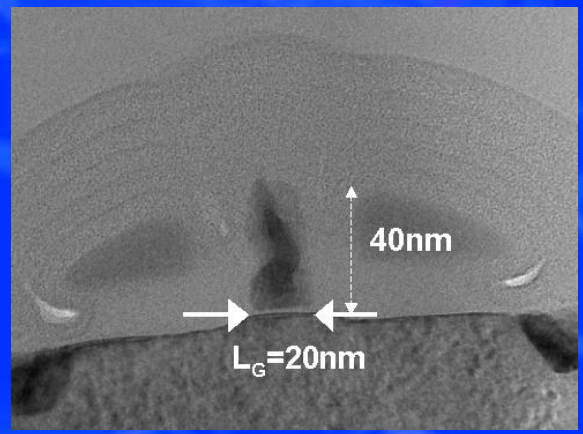
Record small transistors produced in Intel Labs

30 nm



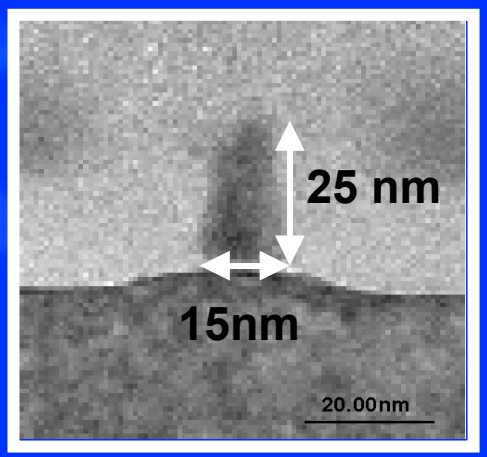
December 2000

20 nm



June 2001

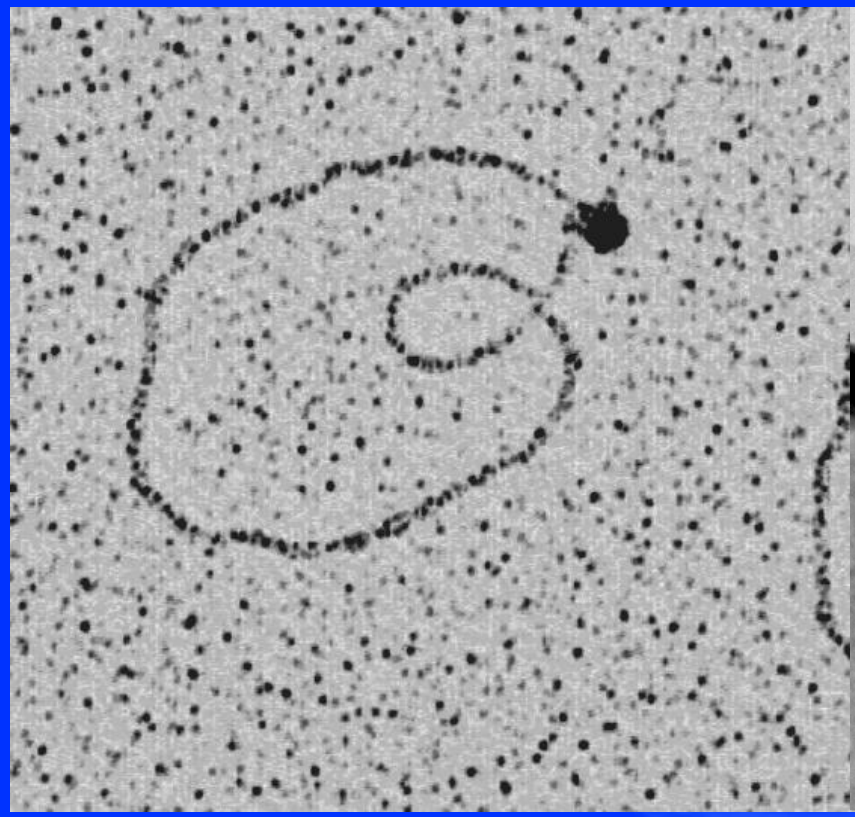
15 nm



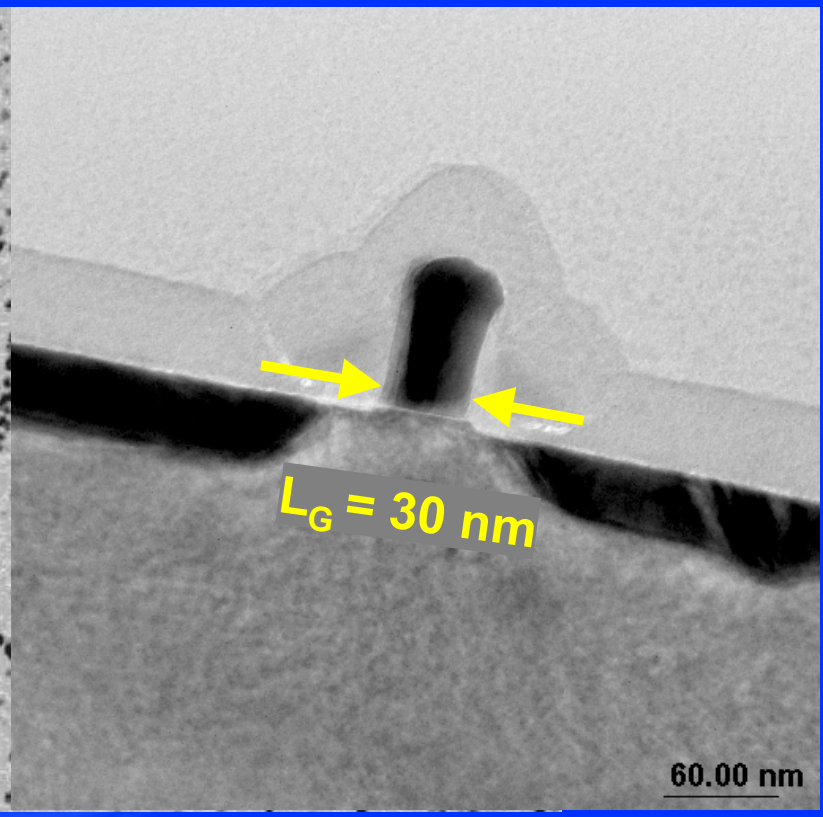
December 2001

Intel Labs

Transistors as Small as DNA

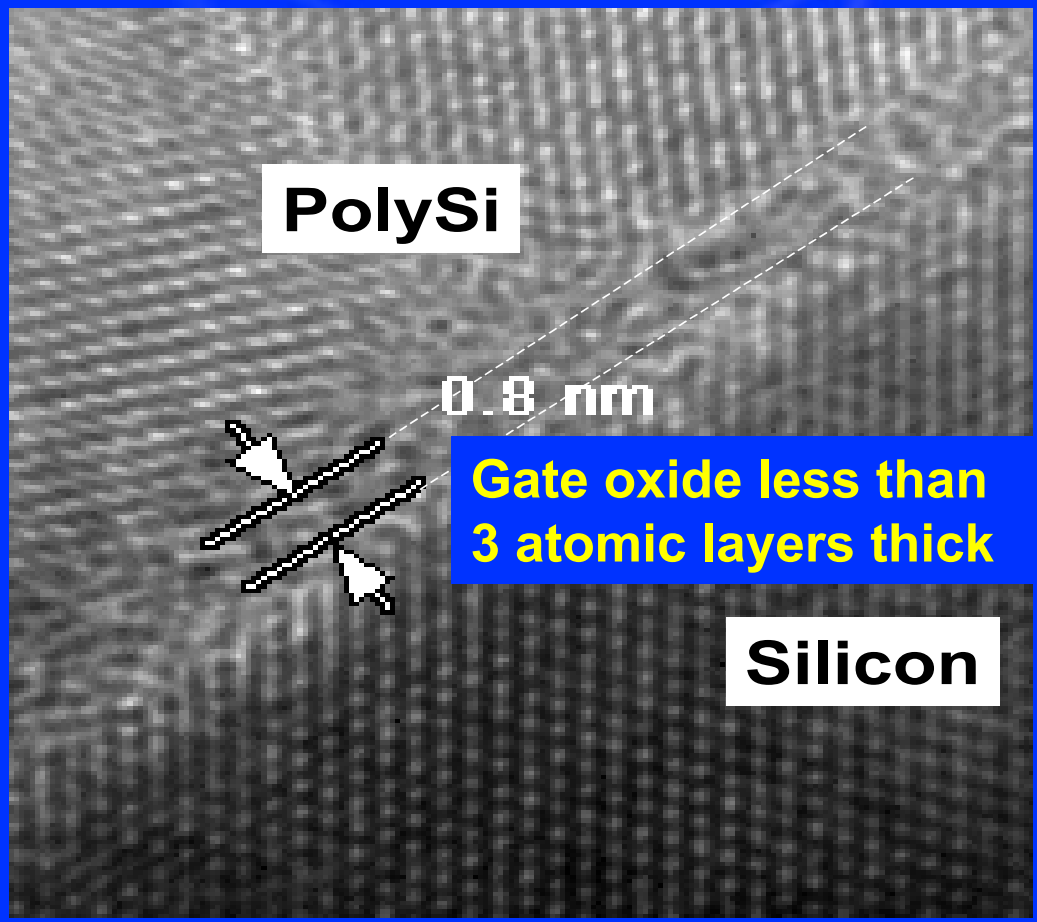


10 nm gold particle attached to Z-DNA antibody
[John Jackson & Inman. *Gene* 198984-226]

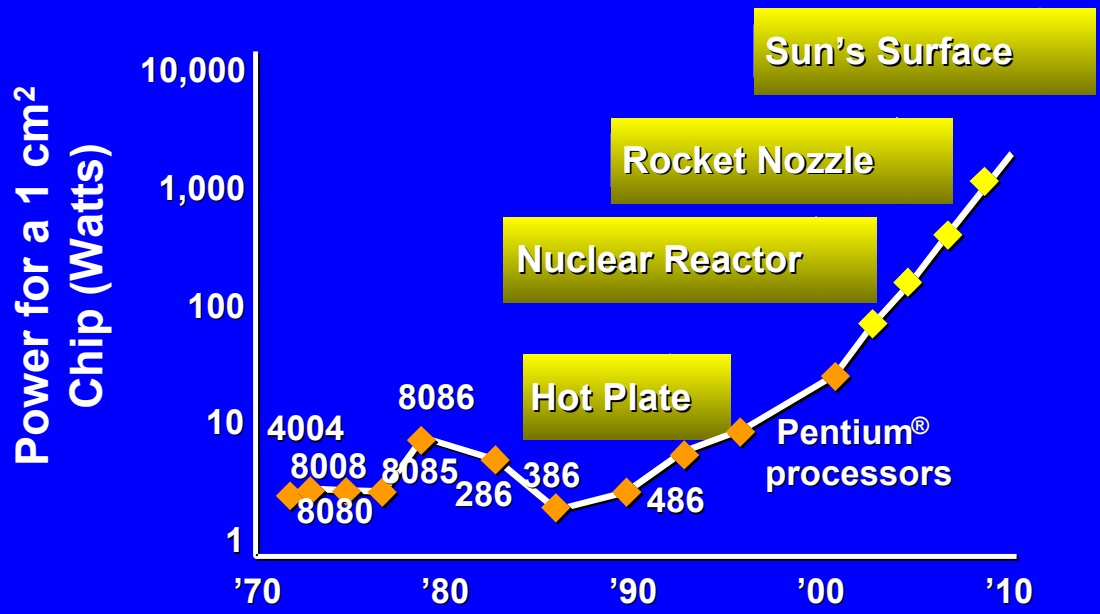


30 nm gate length (L_G=30)
Intel Research Transistor

Gate Oxides as Thin as Atoms



A Big "New" Problem



Pat Gelsinger's Slide from ISSCC 2001

If nothing is done to reduce power,
Moore's Law will be at risk

Transistor Challenge

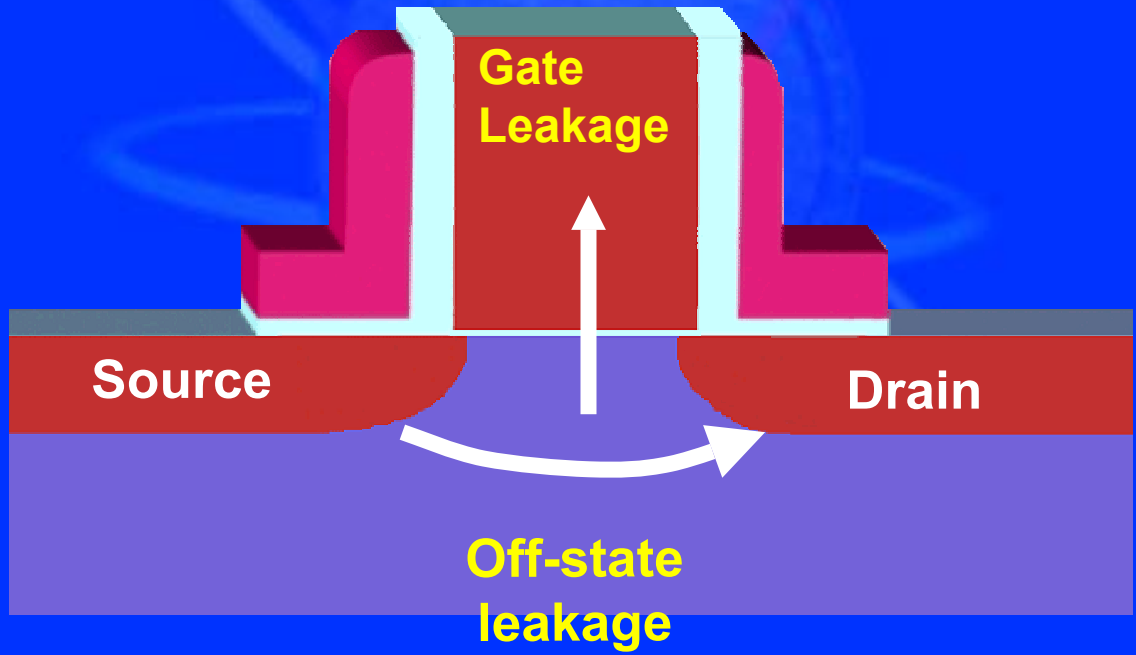
- Continue Moore's Law without Exponential increase in Power Consumption
- Intel introduced two important technologies at IEDM :

  Depleted Substrate Transistors

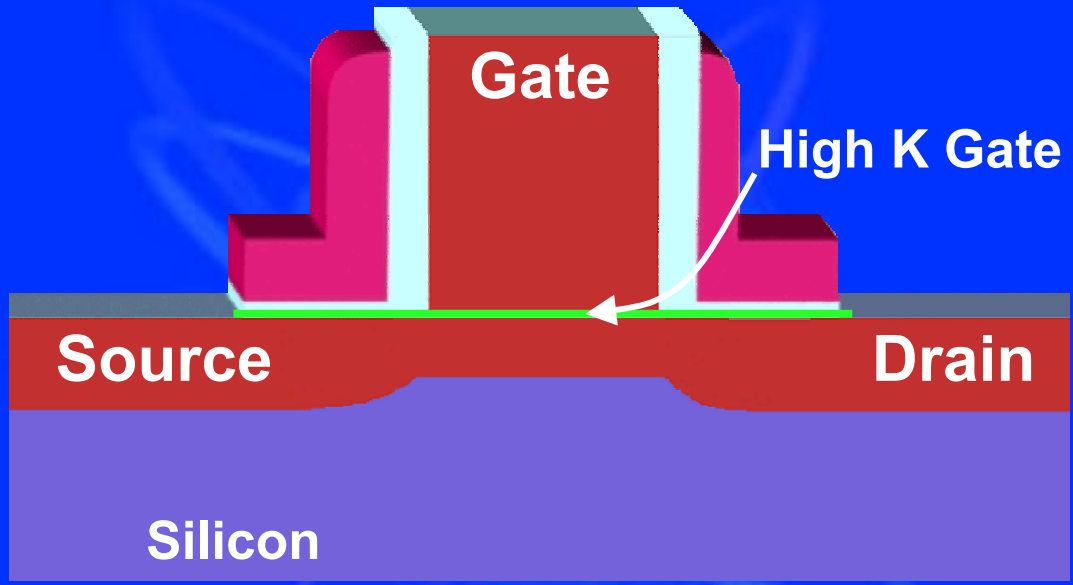
  High K gate dielectric
- Our long term approach is called:

  TeraHertz Transistors

Current Leakage is a Major Problem



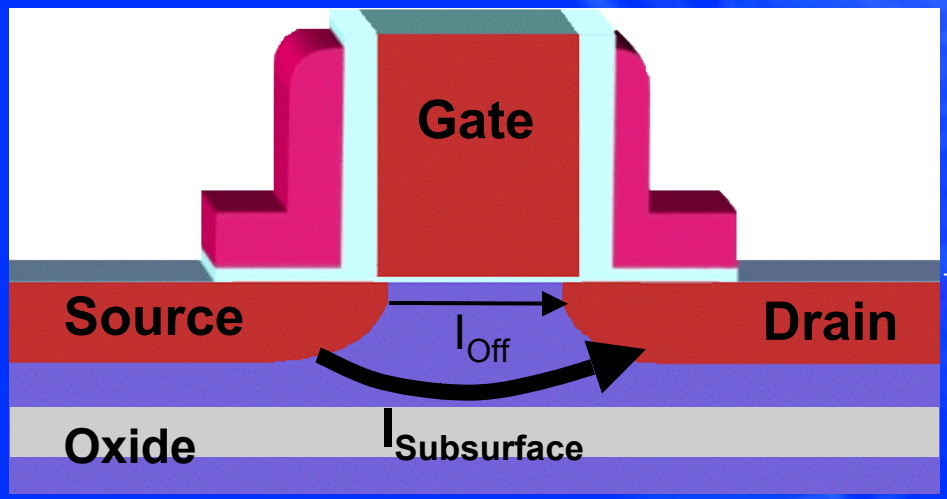
Gate Leakage Solution -- High K Gate Dielectric

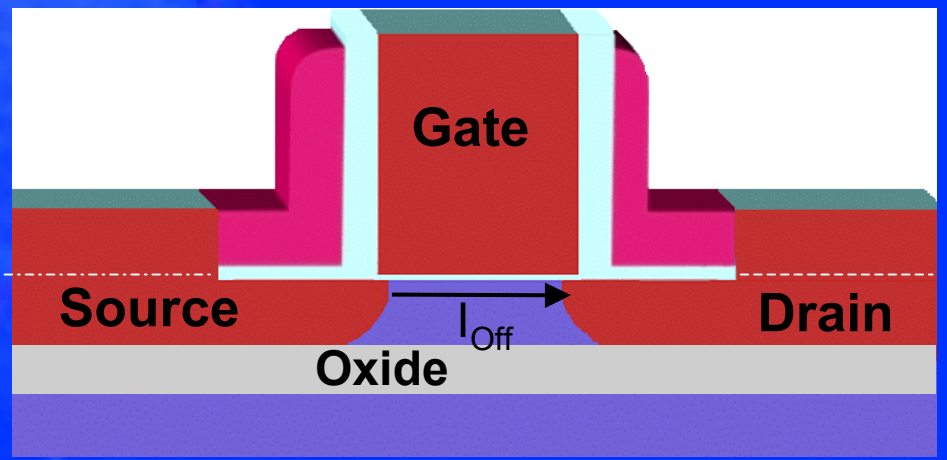


High K gate dielectric

- New material replaces silicon dioxide
- 10,000x lower leakage current through gate dielectric

DST Eliminates Leakage Paths Through Substrate

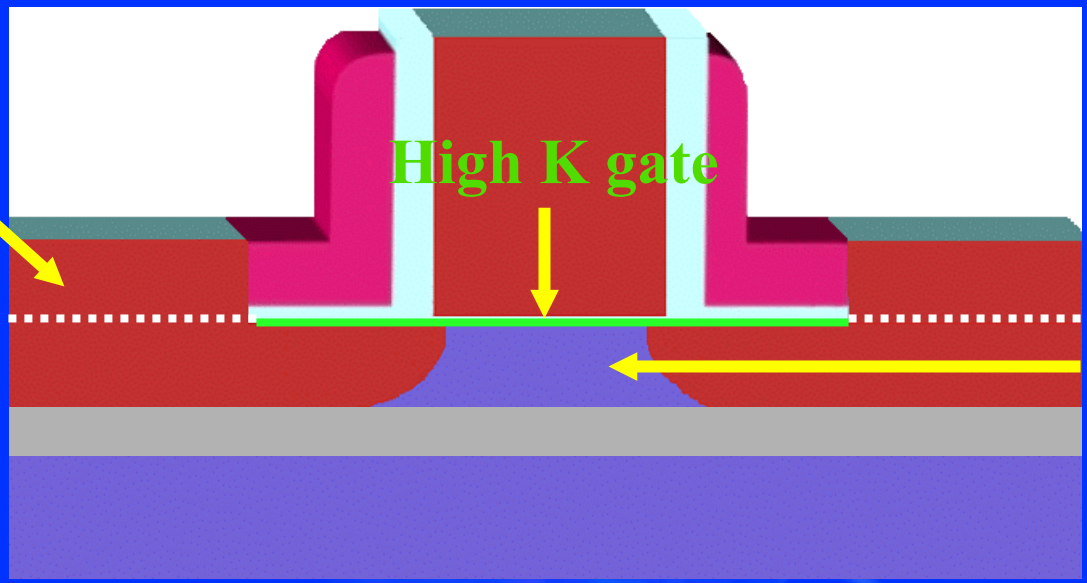




Partially Depleted SOI **DST**

PD SOI has same Ioff performance as bulk Silicon

TeraHertz Transistor Architecture



- 10,000X reduction in gate leakage
- 100X reduction in subthreshold leakage
- Eliminates floating body effect
- Minimizes soft error rates
- 50% lower junction capacitance than PD SOI

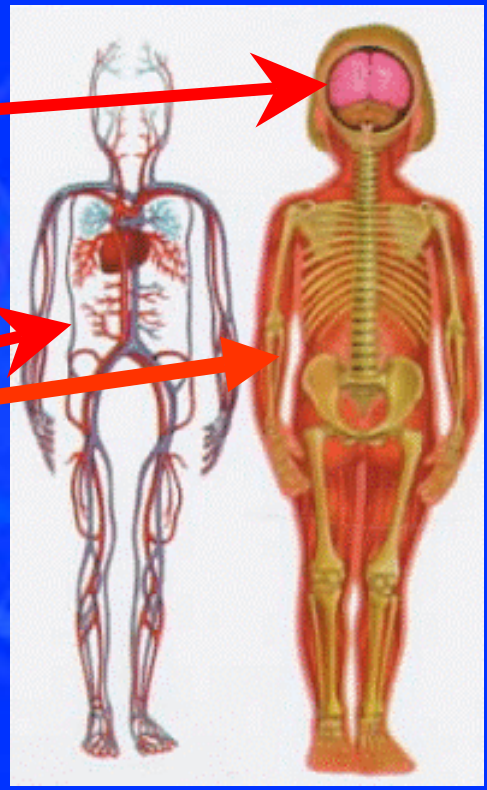
Transistors

- Transistors drive IC performance
  - Transistor progress has accelerated
  - Intel has highest performance transistors in manufacturing and research
- We have not found a device physics limit to making smaller and faster transistors
  - Power, not speed is the issue for this decade

Why is packaging important?

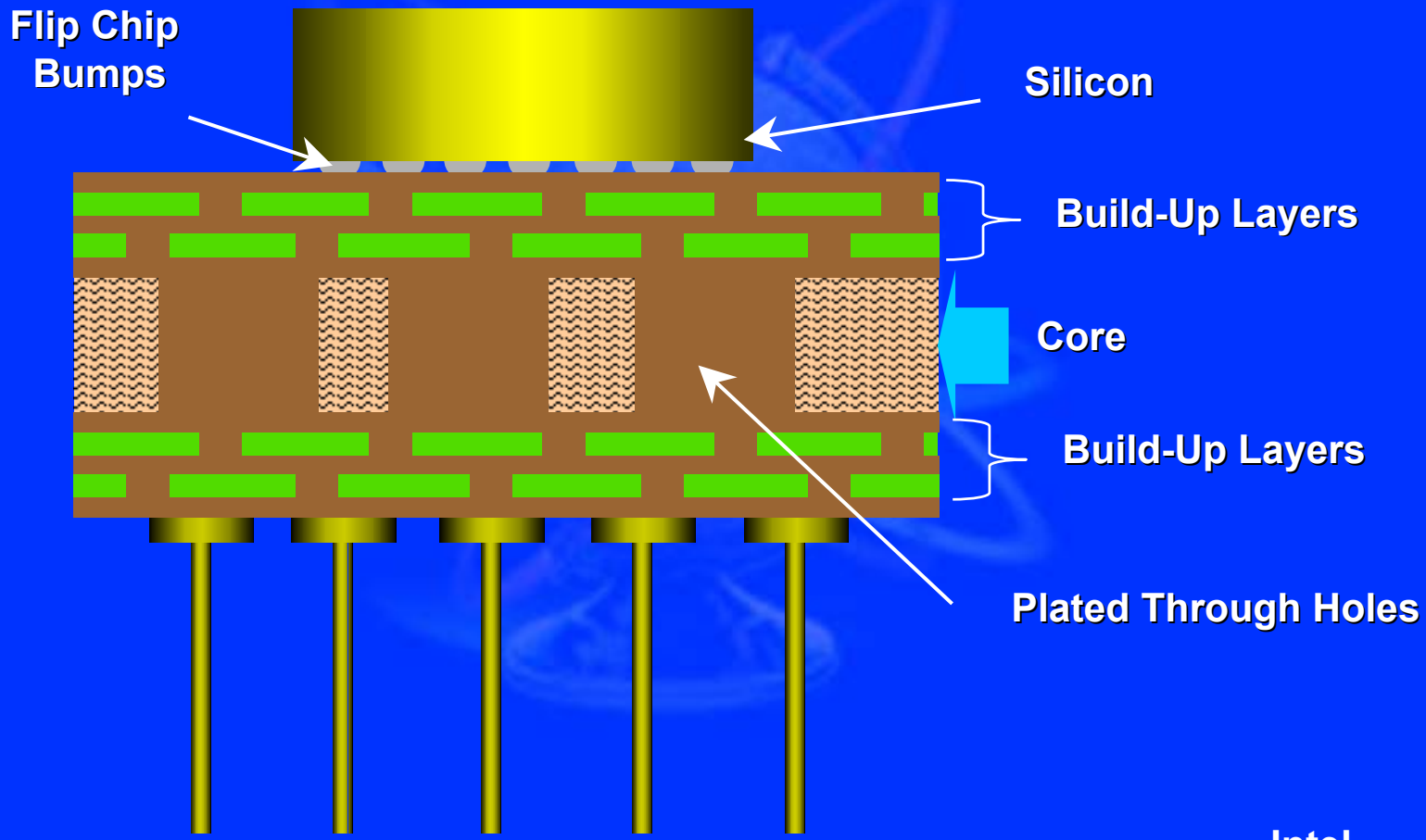
Silicon Processor:
The "brain" of the computer

Packaging:
The rest of the body



Putting Fast Silicon in a Slow Package is like Putting a V-8 Engine in a Yugo

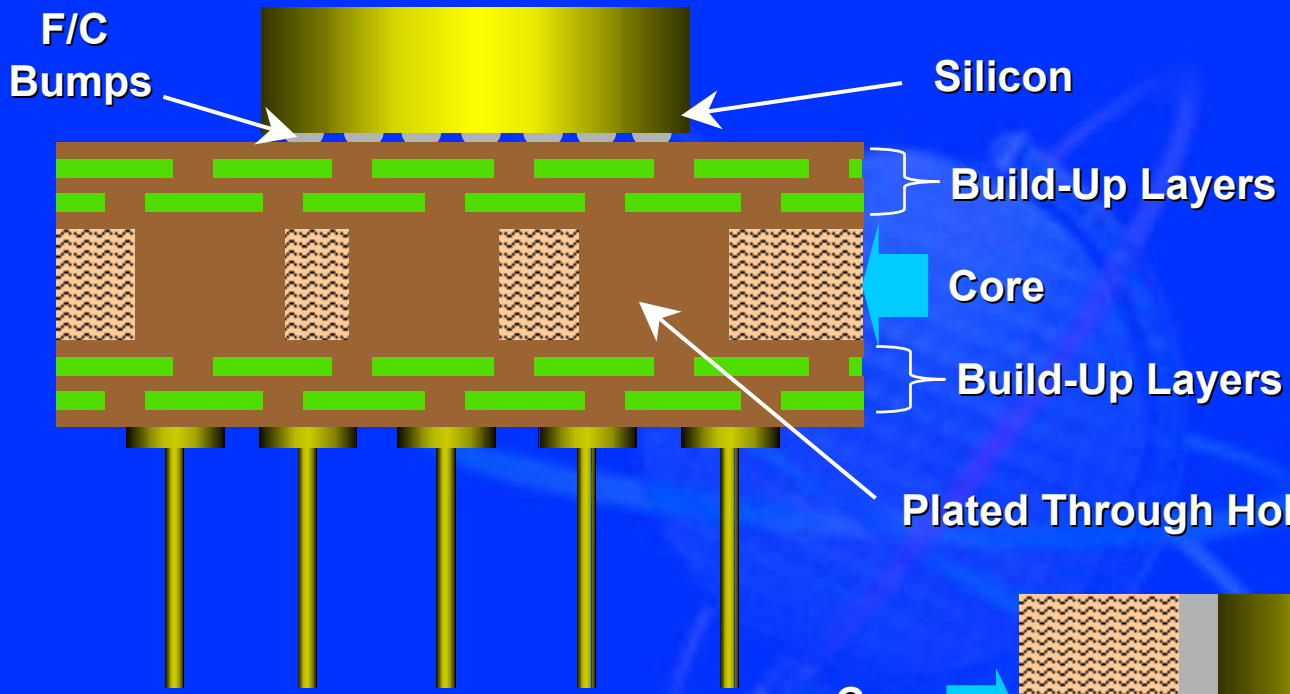
Today's Microprocessor Package



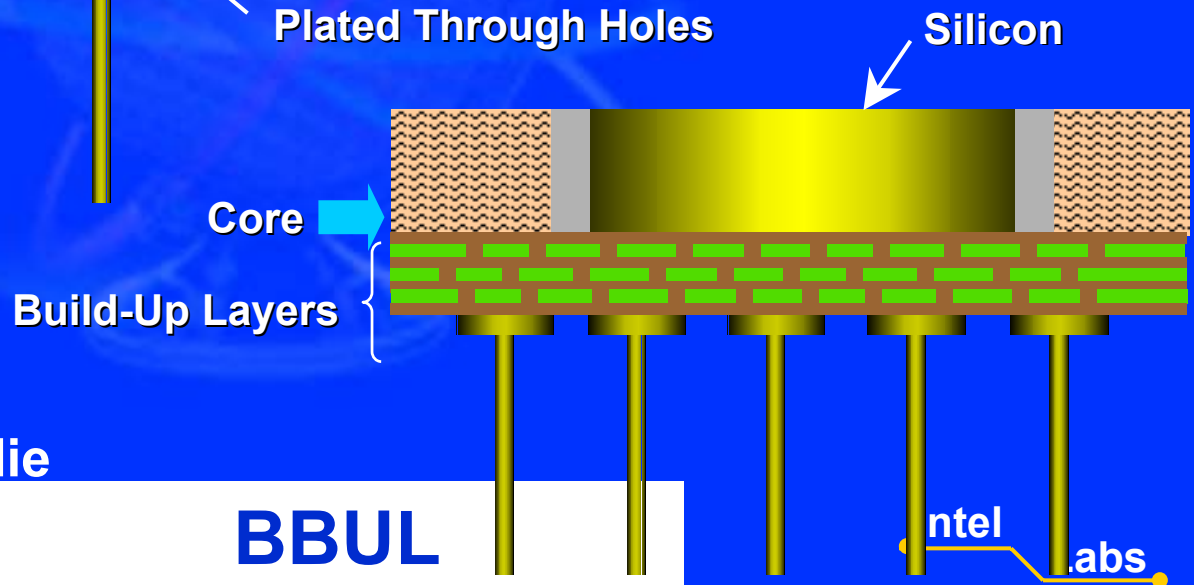
What is BBUL?

- Bumpless Build-Up Layer
- A novel packaging technology
  - Die embedded in package, not attached to its surface
  - Electrical connection between die and package made with copper lines, not C4 solder bumps
- Key advantages:
  - Thinner and lighter than today's packages
  - Higher performance
  - Allows incorporation of multiple silicon components in single package
  - Can help lower power

Today's Package vs. BBUL



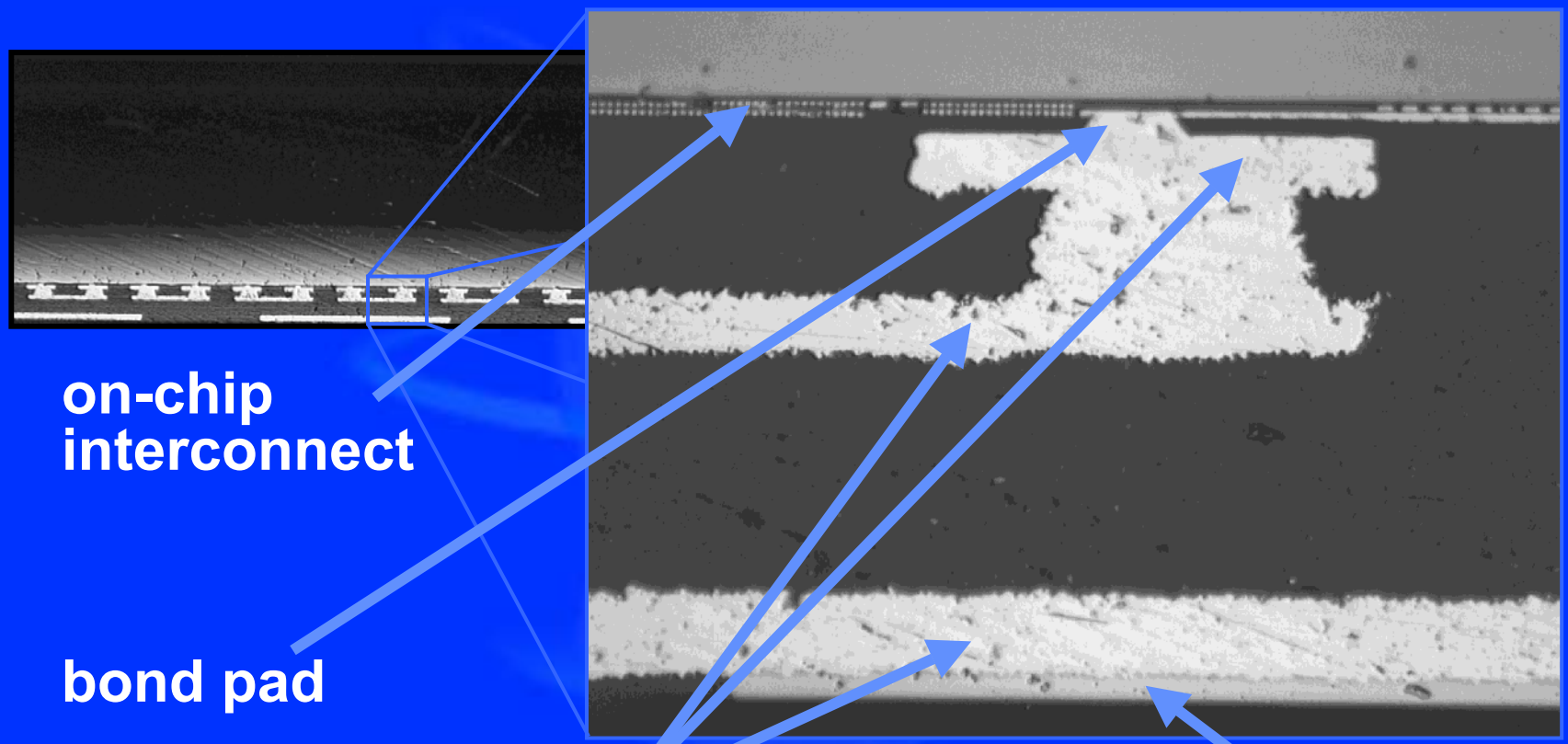
Current Technology



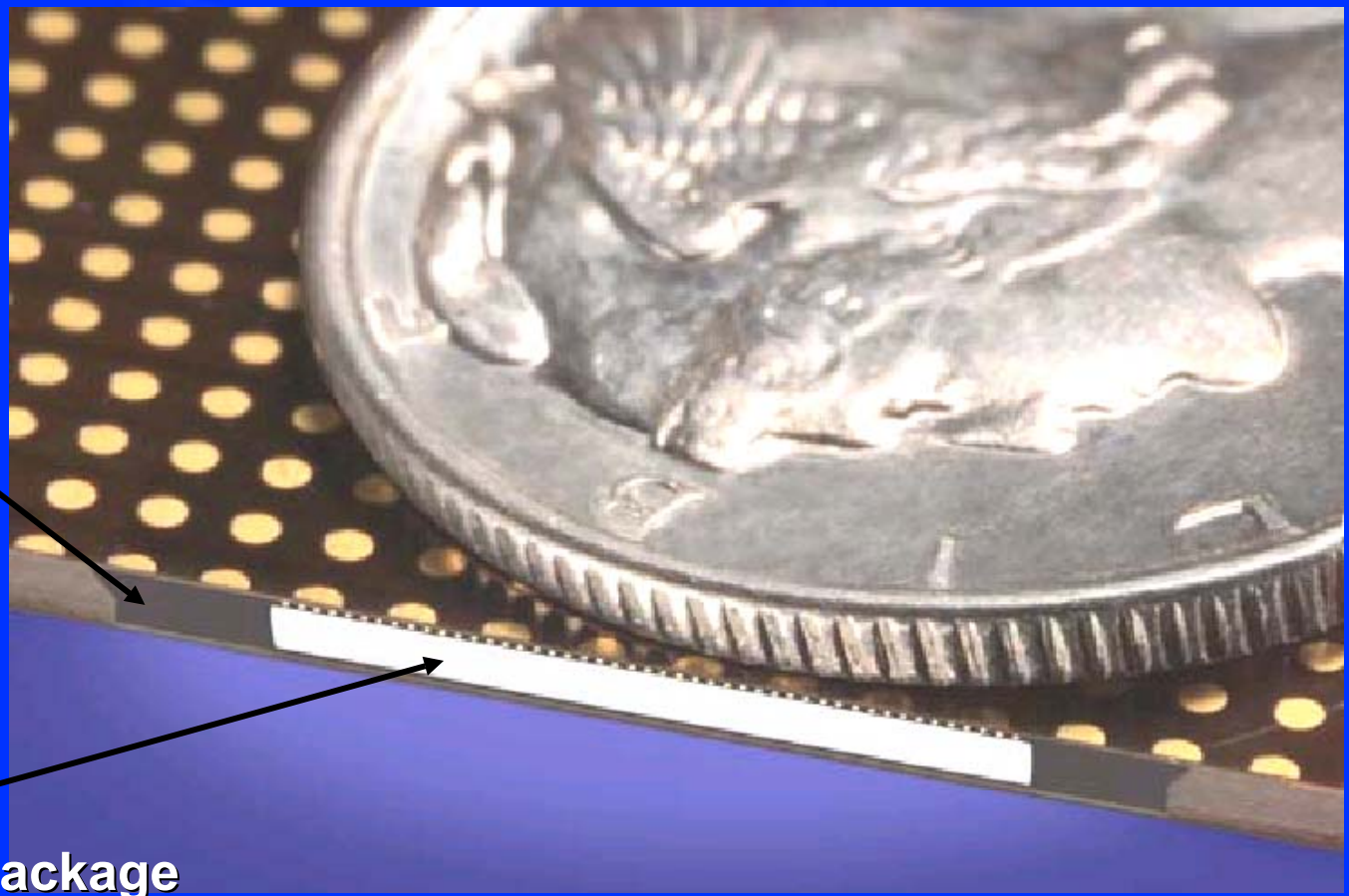
- No solder bumps
- Smaller pad area
- Interconnect on top of die
- Much thinner

BBUL
Die embedded in package

BBUL package cross section

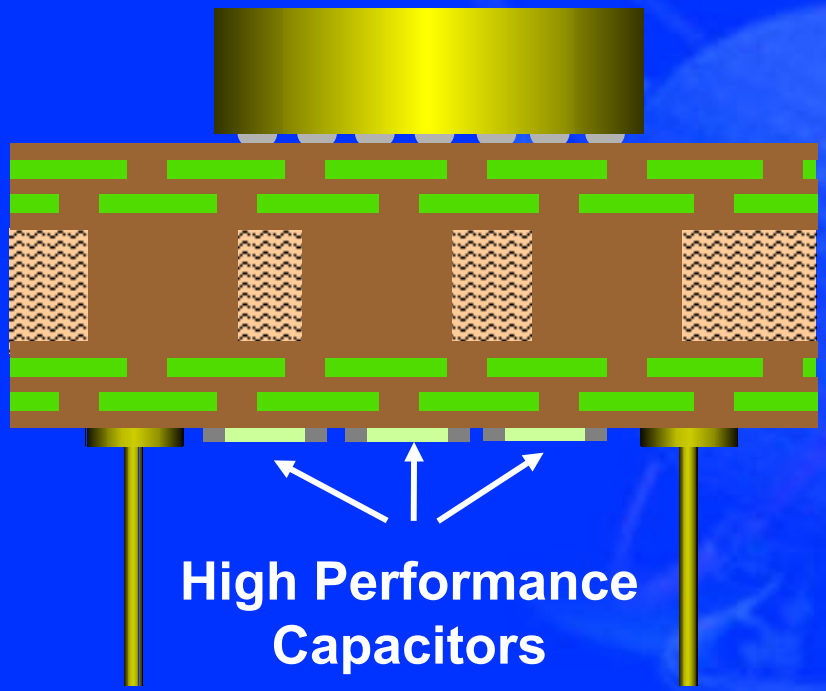


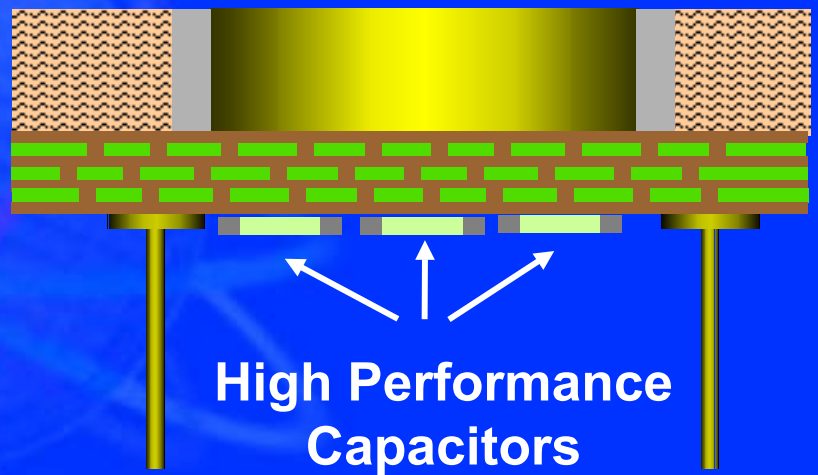
BBUL package thinner than a dime



Note: This package has no pins

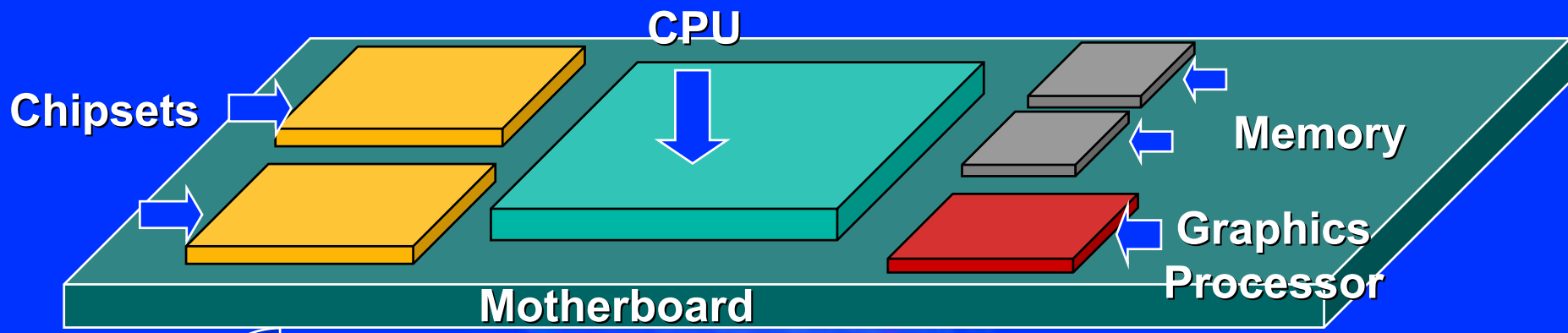
Capacitor Placement Allows Power Delivery Advantage



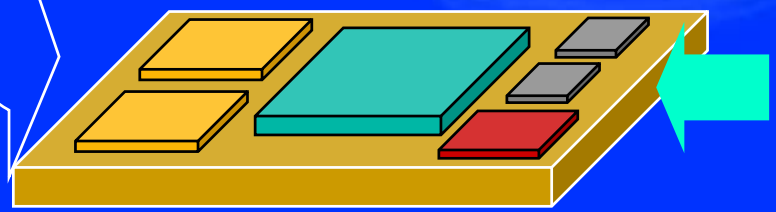


Capacitors can be placed much closer to the die – delivering power where its needed

System-on-a-Package potential



Potential to be used to create "system-on-a-package" designs



What is the significance of BBUL?

- Research demonstration of a novel embedded die package
  - High performance
  - Thinner
  - Enhanced power delivery
  - Compatible with advanced interconnects
  - Multi-chip packaging potential
- Embedded die packaging will emerge in 2nd half of this decade

Summary

- We still have not found a fundamental barrier to Moore's Law
  - Silicon scaling will continue through the end of this decade
  - There will be a new generation every two years
- New materials and new structures are required
  - Lithography
  - Transistors
  - Interconnects
  - Packaging

For more info on Intel's silicon technology, check out the *Silicon Showcase* at

www.intel.com/research/silicon